

Inventec Corporation

R&D Division

Board name : Mother Board Schematic

Project : M11D (Santa Rosa)

Version : 0.1

Initial Date : March 22 , 2007

Inventec Corporation	
<OrgAddr> Inventec Building, 66 Hou-Kang Street Shin-Lin District, Taipei 111, Taiwan TEL: +886-2-2661-0721	
File	
Size C	M11D (Merom+Crestline+ICH8M)
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Schematic Page Description

Santa Rosa Schematic Ver : 0.1

1. Title

2. Schematic Page DESCR

3. Block Diagram

4. Annotations

5. Schematic Modify

6. Timing Diagram

7. DDRII Layout Guideline

8. Merom Processor(1/2)

9. Merom Processor(2/2)

10. CPU Core Power

11. CPU Thermal

12. Crestline Host(1/6)

13. Crestline DMI/Graph(2/6)

14. Crestline DDRII(3/6)

15. Crestline Power(4/6)

16. Crestline Power(5/6)

17. Crestline Ground(6/6)

18. Clock Generator

19. DDRII SDRAM SO-DIMM0

20. DDRII SDRAM SO-DIMM1

21. ICH8M CPU/IDE/SATA(1/4)

22. ICH8M PCI/PCIE/DMI/USB(2/4)

23. ICH8M GPIO(3/4)

24. ICH8M Power/GND(4/4)
25. LCD / CRT

26. DVI / TV-OUT

27. SATA / ODD / Docking

28. MiniCard / NewCard

29. LAN (88E8055B0)

30. USB / CardReader

31. KBC ITE8512F

32. Audio Codec ALC262/AMP

33. Audio MIC / Super I/O

34. Board CON

35. Adaptor in/Charge

36. Dual Battery

37. 5VLA/5VA/3VA

38. 3VS/5VS/1.25VS/1.05VS

39. 1.5VS/1.8V

40. GPU_Core

41. Audio Board

42. USB Board

43. Glidepad Board

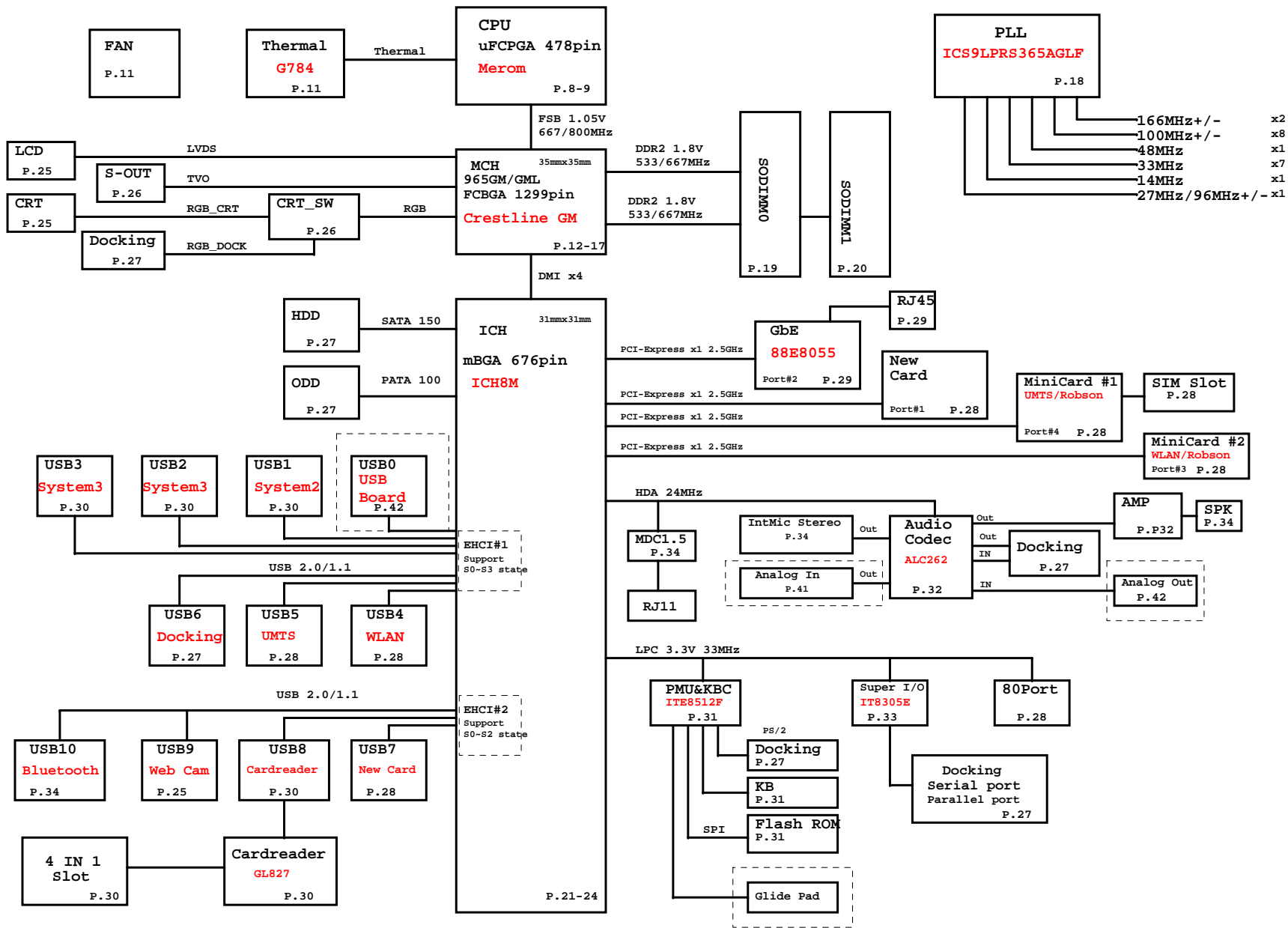
PCI & IRQ & DMA Description :

IDSEL	CHIP	PCIINT	CHIP	BUSMASTER	REQ	CHIP

USB & PCI-Express Description :

USB	DEVICE	USB	DEVICE	PCI-E	DEVICE	PCI-E	DEVICE
Port 0	System	Port 5	Docking	Port 1	Express Card	Port 6	None
Port 1	System	Port 6	Express Card	Port 2	LAN		
Port 2	System	Port 7	Card Reader	Port 3	Mini Card(WLAN)		
Port 3	System	Port 8	Web Cam	Port 4	Mini Card(3G)		
Port 4	Mini Card(3G)	Port 9	Bluetooth	Port 5	None		

System Block Diagram :



4. Net name Description :

Voltage Rails

DCIN	Primary DC system power supply
+5VLA	5.0V always on power rail by LATCH or ACIN
+5VA	5.0V always on power rail by ECPWON
+3VA	3.3V always on power rail by ECPWON
+5VS	5.0V switched power rail by SLP_S3#_3R
+3VS	3.3V switched power rail by SLP_S3#_3R
+1.8VS	1.8V switched power rail by SLP_S3#_3R
VCC_CORE	Core Voltage for CPU
+1.05VS	1.05V power rail for AGTL+ termination/Core for GMCH by SLP_S3#_3R
+1.25VS	1.25V switched power rail by SLP_S3#_3R
+1.5VS	1.5V power rail for CPU PLL/DMI;PCIE;DDRII DLLs for GMCH/Core;PCIE for ICH8m by SLP_S3#_3R
+1.8V	1.8V power rail for DDRII by SLP_S5#_3R
0.9VDDT_DDRII	0.9V DDRII Termination Voltage by SLP_S3#_3R

Part Naming Conventions

- C = Capacitor
- CN = Connector
- D = Diode
- F = Fuse
- L = Inductor
- Q = Transistor
- R = Resistor
- RP = Resistor Pack
- U = Arbitrary Logic Device
- Y = Crystal and Osc

Net Name Suffix

- # = Active Low signal

5. Board Stack up Description

PCB Layers

Layer 1		Component Side, Microstrip signal Layer
Layer 2		Ground Plane
Layer 3		Stripline Layer
Layer 4		Power Plane
Layer 5		Power Plane
Layer 6		Stripline Layer
Layer 7		Ground Plane
Layer 8		Solder Side, Microstrip signal Layer

	Differential Impedance for Microstrip(5-mils)	Differential Impedance for Stripline(4-mils)
Host Clock	95 ohm +/- 20%	100 ohm +/- 20%
PCI-E Clock	95 ohm +/- 20%	100 ohm +/- 20%
DDR2 CLK	70 ohm +/- 20%	70 ohm +/- 20%
DDR2 Strobe	85 ohm +/- 20%	90 ohm +/- 20%
DMI Bus	95 ohm +/- 20%	100 ohm +/- 20%
PCIE Bus	95 ohm +/- 20%	100 ohm +/- 20%
SDVO	95 ohm +/- 20%	100 ohm +/- 20%
SATA	95 ohm +/- 20%	100 ohm +/- 20%
USB	90 ohm +/- 20%	95 ohm +/- 20%
LVDS		100 ohm +/- 20%
Lan	95 ohm +/- 20%	100 ohm +/- 20%

Power Rail	Destination	Voltage	S0 Current
VCC_CORE	Merom HFM: LFM:	1.3319V-1.4375V-1.4591V 0.9221V-0.9625V-0.9739V	36A
+1.05VS	Merom: AGTL+ termination 965GM: Core 965GM: AGTL+ termination ICH8m:	0.997V-1.05V-1.102V 1.0V-1.05V-1.1V 0.9475V-1.05V-1.1025V	2.5A 4.6A 1.4A
+1.5VS	Merom PLL 965GM: PCIE 965GM: LVDS 965GM: TVDAC 965GM: Various PLLs analog supply 965GM: DDR DLLs,DDRII,FSB HSIO ICH8m: ICH8m: ICH8m: ICH8m: Mini Card: Express Card:	1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V	120mA 1.5A 60mA 24mA 320mA 1.885A
+1.8V	965GM: DDRII System Memory SO-DIMM:	1.7V-1.8V-1.9V	3.1A
0.9VDDT_DDRII	DDRII:DDRII Terminator:	0.855V-0.9V-0.945V	1.0A
+2.5VS	965GM: PCIE analog 965GM: LVDS analog 965GM: LVDS I/O 965GM: CRT DAC	2.32V-2.5V-2.625V 2.375V-2.5V-2.625V 2.375V-2.5V-2.625V 2.32V-2.5V-2.625V	2mA 10mA 60mA 70mA
+3VS	965GM: HV CMOS 965GM: TVDAC analog ICH8m: ICH8m: ICH8m: ICH8m: ICH8m: Mini Card: UMTS Express Card: CLK Generator: ICS9LPRS365AGLF Mini Card: WirelessLan Bluetooth: Super I/O: IT8305E Azalia Codec: ALC262 Azalia MDC: HDD: SATA	3.135V-3.3V-3.465V 3.135V-3.3V-3.465V	40mA 120mA
		3.135V-3.3V-3.465V	400mA
		3.0V-3.3V-3.6V	
1.8VS	DVI: SiI1364		
+3VA	Thermal Sensor: Lan: Marvell 88E8055B0 Azalia MDC: EC: ITE8512F ICH8m: RTC Flash ROM: BIOS LCD:	3.0V-3.3V-3.6V	1.0A
+5VS	Cardreader: GL827 Azalia Codec: ALC262 FAN: HDD: SATA ODD: PATA Audio AMP: G1432 Woofer AMP: None Inverter:	3.0V-3.3V-3.6V 4.75V-5.0V-5.25V 4.75V-5.0V-5.25V	Max: 1.0A ; R/W: 460mA ; STDBY: 70mA Max: 1.8A ; R/W: 900mA ; STDBY: 45mA
+5VA	USB: x 3 ports	5VA	1.5A
+5VLA	Control Power		

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M11D (Merom+Crestline+ICH8M)

ANNOTATIONS

Schematic modify Item and History :

V0.1 First release

V0.1 to AX1

- 1.For FAN PWM Control
Change C259 From 0.01uF to NU
Change C538 From 1uF to NU
Change R118 From 47Kohm to 1Kohm
Change R119 From 4.7Kohm to 0 ohm
Change R415 From 10 ohm to NU
- 2.For Power sequence issue (VRMPWRGD From CORECLK_EN Change to VCORE_GD)
Change R131 From NU to 0 ohm
Change R133 From 100K ohm to NU
Change U13 From TC7SZ04FU to NU
- 3.For Power sequence issue (Delay VCORE_GD to PM_ICH_PWROK)
ADD C1202 to 0.1uF
ADD R1116 to 100K ohm
ADD D34 BAT54C-7
- 4.For VESA Specification Requirement (MB Side)
Change C5,C6,C8 From 22pF to 18pF
Change L3,L4,L5 From 17ohm 600mA to 10ohm 500mA
Change C9,C10,C11 From 10pF to NU
Change R4,R5,R6 From 200ohm to 220ohm
- 5.For VESA Specification Requirement (Docking Side)
Change R266,R267,R268 From 200ohm to 220ohm
- 6.For Serial RING Wake (Change from to EC)
Change RING# single connect to U9 IT8512E Pin119
Change U4 MAX3243 Pin26 From 3VS to 3VA
- 7.For Audio
Change Speaker single change connect to pin35,36
Change Headphone single change connect to pin39,41
Change R586 From 5.1Kohm to 39.2Kohm
DEL R584,R580,R588,R589,C679,U46
- 8.For EMI Requirement
ADD C1206~C1251 0.1uF in 3VA,5VA,DCIN,VADPTR_DOCK
ADD C1204,C1205 1000pF in SW Board connecter
ADD L1105~L1108 in Speaker connecter
Change Q29,Q30,Q32,Q33 From FDS6676AS to FDMS8670S
ADD C1252~C1254 0.1uF in USB_VCC1
- 9.For SATA Eye issue
Change C587,C591 From 3300pF to 3900pF
- 10.For Docking DVI

TX2 Change to CN28 Pin 13,14
TX1 Change to CN28 Pin 16,17
TX0 Change to CN28 Pin 19,20
TXC Change to CN28 Pin 22,23

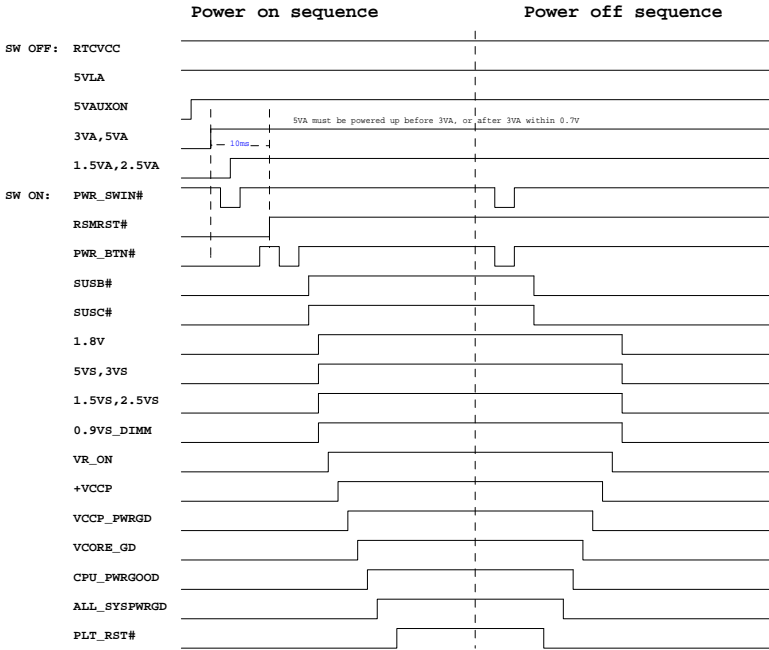
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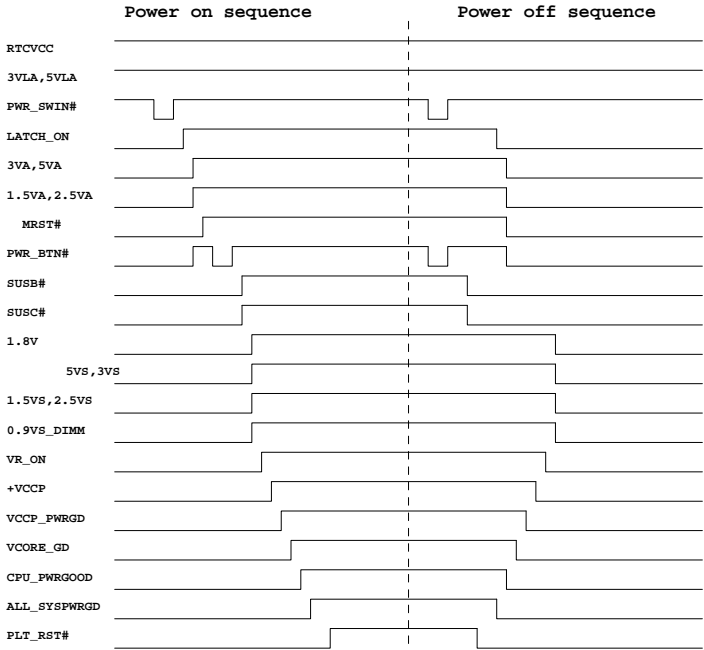
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Date:	Friday, June 01, 2007	Sheet	5 of 43

SYSTEM POWER ON/OFF SEQUENCE

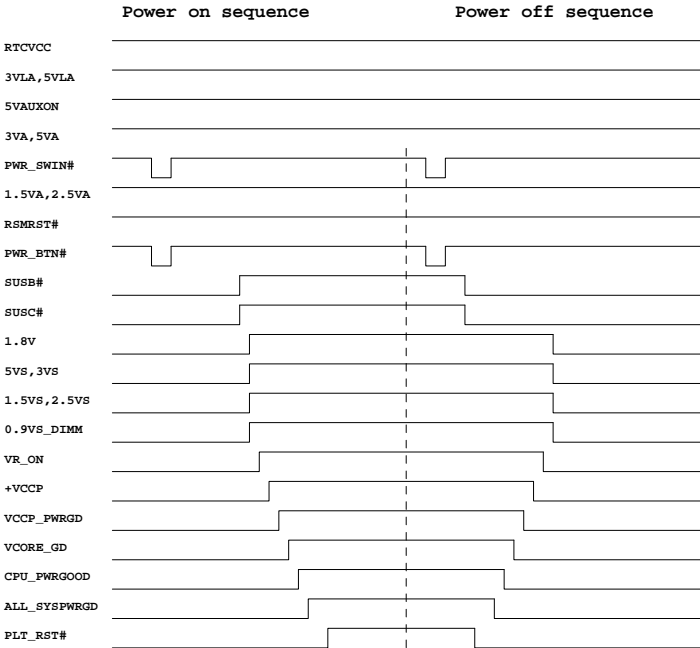
Power on/off sequence AC insert(First)



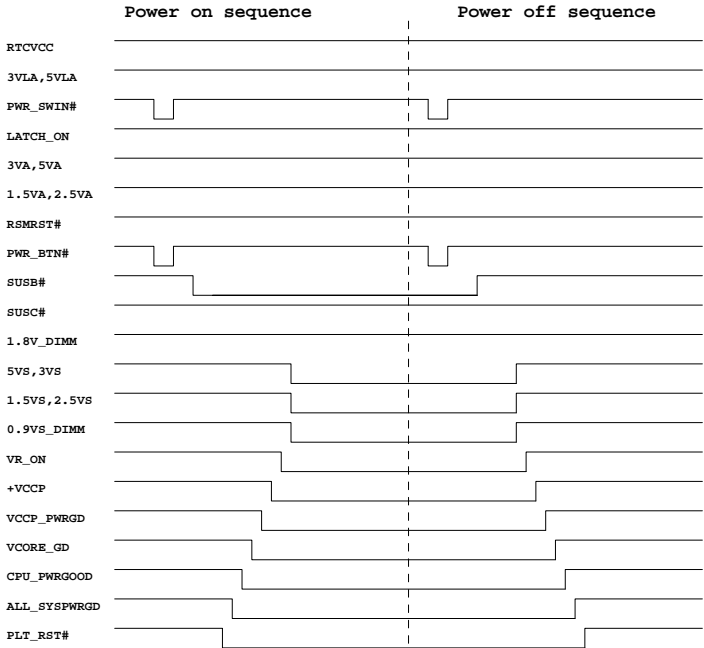
Battery only Power on/off sequence



Power on/off sequence AC insert(S4)



Suspend resume sequence(S3)



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File: M11D (Merom+Crestline+ICH8M)
Size: Custom
Document Number: AX1
Date: Friday, June 01, 2007
Sheet: 6 of 43
Timing Diagram

DDRII Layout Guideline :

Crestline DDRII Layout Guidelines

DDRII Signal Groups

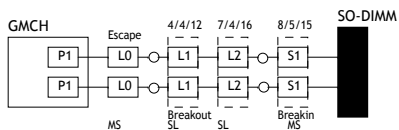
Group Signal Name

Data	M_A_DQ[63..0]/M_B_DQ[63..0] M_A_DM[7..0]/M_B_DM[7..0] M_A_DS[7..0]/M_B_DS[7..0] M_B_DQS[7..0]/M_B_DQS[7..0]
Address	M_A_A[13..0]/M_B_A[13..0] M_A_RAS#/M_B_RAS# M_A_CAS#/M_B_CAS# M_A_WE#/M_B_WE#
Control	M_CS#[3..0] M_CKE[3..0] M_ODT[3..0]
Clock	M_CLK_DDR[3..0] M_CLK_DDR#[3..0]
FeedBack	SA_RCVEN#/SB_RCVEN#

Length Matching and Length Formulas

Signal Group	Minimum Length	Maximum Length
Control-to-Clock	Clock - 1.0"	Clock - 0.0"
Command-to-Clock	Clock - 1.0"	Clock + 1.0"
Strobe-to-Clock	Clock - 0.5"	Clock + 1.0"
Data-to-Strobe	Strobe - 220mils	Strobe - 180mils

CLK group : M_CLK_DDR[3..0],M_CLK_DDR#[3..0]



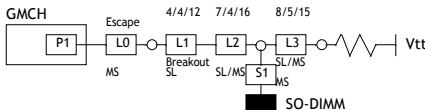
Topology	Differential Pair Point-to-Point
Reference Plane	Ground
Single Ended Trace Impedance	42 +/- 15%
Differential Mode Impedance	70 +/- 20%
Minimum Serpentine Spacing	Inner Layer : 12 mils Outer Layer : 15 mils
Package Length Range - P1	350 mils - 625 mils
Min. Serpentine Spacing	25 mils
Trace Length Limit - L0 (MS)	Nominal Trace Width : 5mils, 4mils Length Limit: Max = 50 mils (Escape) Min. Trace Spacing : 5mils, 4mils
Trace Length Limit - L1 (SL) (Breakout length segment)	Length Limit: Max = 700 mils Nominal Trace Width : 4mils Min. Trace Spacng (pair) : 4mils Min. Trace Spacng (Other) : 12 mils
Stub Length S1-Stub from via to SO-DIMM	Max = 200 mils (Breakin)
MB Length Limits - L0 + L1 + L2 + S1	Min = 500 mils Max = 4000 mils
Total Length - P1 + L0 + L1 + L2 + S1	Max = 4500 mils Total Length for Channel A : X0 Total Length for Channel B : X1
Maximum Via Count	2 (Per side)
SCK to SCK# Length Matching (Total Length including package)	Match total length to within 5 mils
Clock to Clock Length Match (Total Length)	Match Channel A clocks to X0 +/- 20mils Match Channel A clocks to X1 +/- 20mils
Breakout Exceptions (Reduce geometries for GMCH break-out region)	Inner Layer : 4/12 mils to other DDR2 Outer Layer : 5/15 mils to other DDR2 Max. breakout length is 500 mils
Breakin Exceptions (Reduce geometries for SO-DIMM break-in region)	CK to CK# spacing rule waived at connector spacing of 15 mils to other DDR2 Max. breakin length is 200 mils

Feedback group :

SA_RCVENIN#],SA_RCVENOUT#],SB_RCVENIN#],SB_RCVENOUT#]

These signals are routed internally on the GMCH package and don't require any routing on the MB. As a result, can be left as NC.

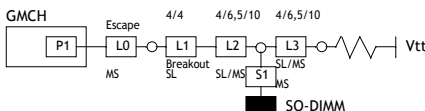
Control group : SM_CKE[3..0],SM_CS#[3..0],SM_ODT[3..0]



Topology	Point-to-Point with parallel termination
Reference Plane	Ground
Characteristic Trace Impedance	55 +/- 15%
Nominal Trace Width	Inner Layer : 4 mils Outer Layer : 5 mils
Minimum CTRL Trace Spacing	Inner Layer : 8 mils Outer Layer : 10 mils
Minimum Spacing to Other DDR2	Inner Layer : 12 mils Outer Layer : 15 mils
Minimum Isolation Spacing to non-DDR2	25 mils
Package Length P1	750 mils +/- 200 mils
Trace Length Limit - L0	Max = 50 mils (Escape)
Trace Length Limit - L1	Max = 500 mils (Breakout)
Stub Length S1-Stub from via to SO-DIMM	Max = 200 mils (Breakin)
MB Length Limits - L0 + L1 + L2 + S1 - From GMCH ball to SO-DIMM pad	Min = 500 mils Max = 4500 mils
Total Length - P1 + L0 + L1 + L2 + S1 - From GMCH die to SO-DIMM pad	Max = 5000 mils
Trace Length L3	Max = 1500 mils
Parallel Termination Resistor	56 +/- 5%
Maximum Via Count	3
CTRL to SCK/SCK# Length Matching (Total Length including package)	(CLK-1.0") <= CTRL <= (CLK-0.0")
Breakout Exceptions (Reduce geometries for GMCH break-out region)	Inner Layer : 4 mils spacing allowed Outer Layer : 5 mils spacing allowed Max. breakout length is 500 mils

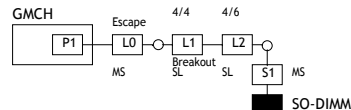
Command group :

SA_MA[13..0],SB_MA[13..0],SA_BS[2..0],SB_BS[2..0],SA_RAS#
SB_RAS#,SA_CAS#,SB_CAS#,SA_WE#,SB_WE#



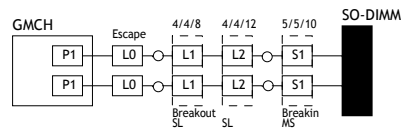
Topology	Point-to-Point with parallel termination
Reference Plane	Ground
Characteristic Trace Impedance	55 +/- 15%
Nominal Trace Width	Inner Layer : 4 mils Outer Layer : 5 mils
Minimum CMD Bus Trace Spacing	Inner Layer : 6 mils Outer Layer : 10 mils
Minimum Spacing to Other DDR2	Inner Layer : 12 mils Outer Layer : 15 mils
Minimum Isolation Spacing to non-DDR2	25 mils
Package Length P1	750 mils +/- 350 mils
Trace Length Limit - L0	Max = 50 mils (Escape)
Trace Length Limit - L1	Max = 500 mils (Breakout)
Stub Length S1-Stub from via to SO-DIMM	Max = 200 mils (Breakin)
MB Length Limits - L0 + L1 + L2 + S1 - From GMCH ball to SO-DIMM pad	Min = 500 mils Max = 4500 mils
Total Length - P1 + L0 + L1 + L2 + S1 - From GMCH die to SO-DIMM pad	Max = 5000 mils
Trace Length L3	Max = 1500 mils
Parallel Termination Resistor	56 +/- 5%
Maximum Via Count	3
CTRL to SCK/SCK# Length Matching (Total Length including package)	(CLK-1.0") <= CMD <= (CLK+1.0")
Breakout Exceptions (Reduce geometries for GMCH break-out region)	Inner Layer : 4 mils spacing allowed Outer Layer : 5 mils spacing allowed Max. breakout length is 500 mils

Data group : SA_DQ[63..0],SB_DQ[63..0],SA_DM[7..0],SB_DM[7..0]



Topology	Point-to-Point
Reference Plane	Ground
Characteristic Trace Impedance	55 +/- 15%
Nominal Trace Width	Inner Layer : 4 mils Outer Layer : 5 mils
Minimum DQ Bus Trace Spacing	Inner Layer : 6 mils Outer Layer : 8 mils
Minimum Serpentine Spacing	Same as DQ-to-DQ routing
Minimum Spacing to Other DDR2	Inner Layer : 12 mils Outer Layer : 15 mils
Minimum Isolation Spacing to non-DDR2	25 mils
Package Length P1	750 mils +/- 350 mils
Trace Length Limit - L0	Max = 50 mils (Escape)
Trace Length Limit - L1	Max = 500 mils (Breakout)
Stub Length S1-Stub from via to SO-DIMM	Max = 200 mils (Breakin)
MB Length Limits - L0 + L1 + L2 + S1 - From GMCH ball to SO-DIMM pad	Min = 500 mils Max = 4500 mils
Total Length - P1 + L0 + L1 + L2 + S1 - From GMCH die to SO-DIMM pad	Max = 5000 mils
Trace Length L3	Max = 1500 mils
Maximum Via Count	2
DQ/DM to DQS Length Matching (Total Length including package)	Match DQ/DM to [SDQS - 200mils] +/- 20mils, per byte lane
Breakout Exceptions (Reduce geometries for GMCH break-out region)	Inner Layer : 4 mils spacing allowed Outer Layer : 5 mils spacing allowed Max. breakout length is 500 mils

Data Strobe group : SA_DQS[7..0],SA_DQS[7..0]#,SB_DQS[7..0],SB_DQS[7..0]#



Topology	Differential Pair Point-to-Point
Reference Plane	Ground
Single Ended Trace Impedance	55 +/- 15%
Differential Mode Impedance	85 +/- 20%
Nominal Trace Width	Inner Layer : 4 mils Outer Layer : 5 mils
Nominal DQS to DQS# Spacing (edge to edge)	Inner Layer : 4 mils Outer Layer : 5 mils
Minimum DQS to DQ Spacing	Inner Layer : 12 mils Outer Layer : 15 mils
Minimum Serpentine Spacing	Inner Layer : 8 mils Outer Layer : 10 mils
Minimum Spacing to Other DDR2	Inner Layer : 12 mils Outer Layer : 15 mils
Minimum Isolation Spacing to non-DDR2	25 mils
Package Length Range - P1	750 mils +/- 350 mils
Trace Length Limit - L0	Max = 50 mils (Escape)
Trace Length Limit - L1	Max = 500 mils (Breakout)
Stub Length S1-Stub from via to SO-DIMM	Max = 200 mils (Breakin)
MB Length Limits - L0 + L1 + L2 + S1 - From GMCH ball to SO-DIMM pad	Min = 500 mils Max = 4500 mils
Total Length - P1 + L0 + L1 + L2 + S1 - From GMCH die to SO-DIMM pad	Max = 5000 mils
Trace Length L3	Max = 1500 mils
Maximum Via Count	2 (Per side)
DQS to DQS# Length Matching	Match total length to within 5 mils
Clock to Clock Length Match (Total Length include package)	(CLK-0.5") <= DQS <= (CLK+1.0")
Breakout Exceptions (Reduce geometries for GMCH break-out region)	Inner Layer : 8 mils to other DDR2 Outer Layer : 10 mils to other DDR2 Max. breakout length is 500 mils
Breakin Exceptions (Reduce geometries for SO-DIMM break-in region)	DQS to DQS# spacing rule waived at connector spacing of 10 mils to other DDR2 Max. breakin length is 200 mils

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AX1

M11D (Merom+Crestline+ICH8M)

DDRII Layout Guideline

Date

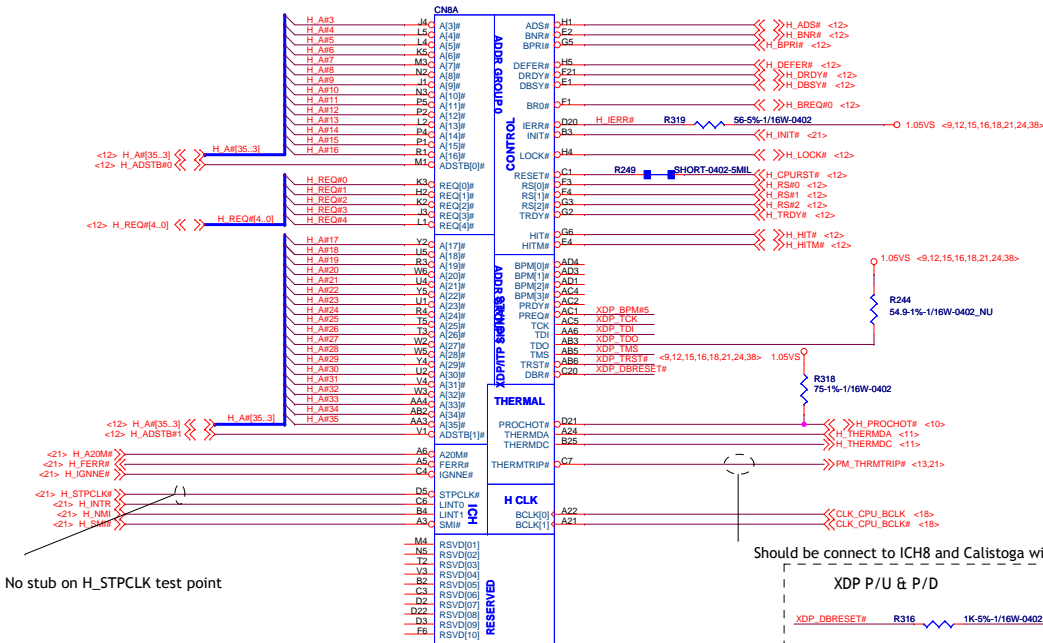
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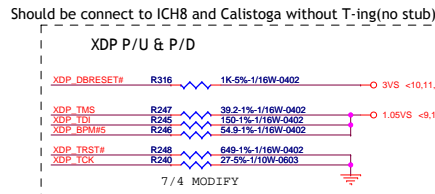
43



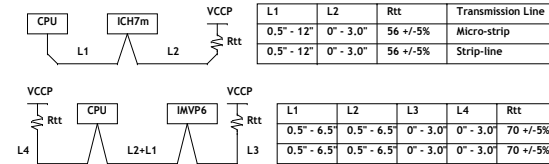
No stub on H_STPCLK test point

Route to TP via and place gnd via w/in 100mils

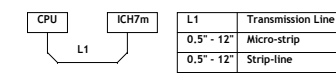
A#[32-39], APM#[0-1]: Leave escape routing on for future functionality



Topology : FERR#



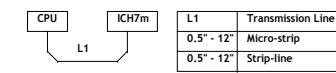
Topology : PWRGOOD



Topology : CPUSLP#



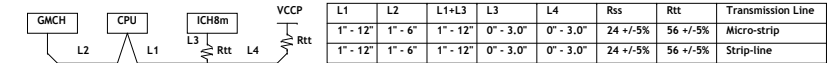
Topology : INTR, NMI, A20M#, DPSLP#, IGNE#, INIT#, SMI#, STPCLK#



Topology : RESET#



Topology : THERMTRIP#



FSB Common Clock Signal Layout Guide :

H_ADS#, H_BNR#, H_BPRI#, H_BRO#, H_DBSY#, H_DEFER#, H_DPWR#, H_DRDY#, H_HIT#, H_HITM#, H_LOCK#, H_RS#[2..0], H_TRDY#, H_CPURST#.			
Transmission Line Type	Total Trace Length	Normal Impedance	Spacing (mils)
Strip-line(Int. Layer)	1.0 - 6.5 inch	55 +/- 15%	W=4 & S=8 mils
Micro-strip(Ext. Layer)			W=5 & S=10 mils

FSB Source Synchronous Data Length Variation and Strobe Matching Requirements :

Signals Name	Signals Matching	Strobes associated with the group	Strobe-to-Strobe Complement Matching
H_D#[15..0], H_DINV#0	+/- 100 mils	H_DSTBP#0, H_DSTBN#0	+/- 25 mils
H_D#[31..16], H_DINV#1	+/- 100 mils	H_DSTBP#1, H_DSTBN#1	+/- 25 mils
H_D#[47..32], H_DINV#2	+/- 100 mils	H_DSTBP#2, H_DSTBN#2	+/- 25 mils
H_D#[63..48], H_DINV#3	+/- 100 mils	H_DSTBP#3, H_DSTBN#3	+/- 25 mils

FSB Source Synchronous Data Signal Routing Topology#1 :

Signal Name	Transmission Line Type	Total Trace Length	Normal Impedance	Width & Spacing (mils)
H_DINV#[3..0]	Strip-line	0.5 - 5.5 inch	55 +/- 15%	W=4 & S=8 mils
H_DATA#[63..0]	Strip-line	0.5 - 5.5 inch	55 +/- 15%	W=4 & S=8 mils
H_DSTBN#[3..0]	Strip-line	0.5 - 5.5 inch	55 +/- 15%	W=4 & S=4 mils
H_DSTBP#[3..0]	Strip-line	0.5 - 5.5 inch	55 +/- 15%	W=4 & S=12 mils

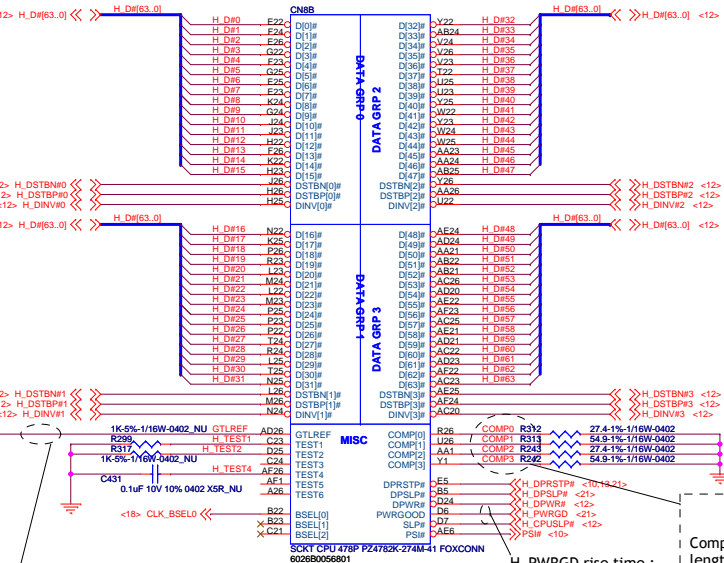
FSB Source Synchronous Address Length Variation and Strobe Matching Requirements :

Signals Name	Signals Matching	Strobes associated with the group	Strobe to Assoc. Address Signal Matching
H_A#[16..3], H_REQ#[4..0]	+/- 200 mils	H_ADSTB#0	+/- 200 mils
H_A#[35..17]	+/- 200 mils	H_ADSTB#1	+/- 200 mils

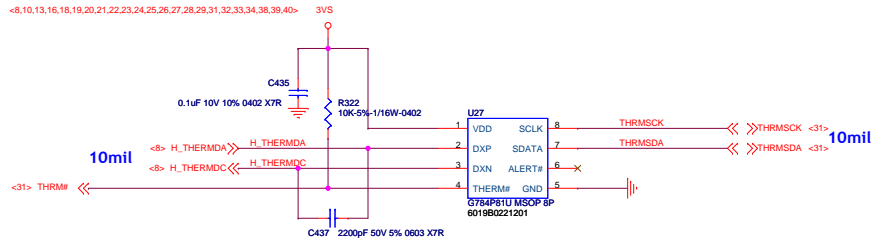
*** No length matching requirements exist between H_ADSTB#0 and H_ADSTB#1

FSB Source Synchronous Address Signal Routing :

Signal Name	Transmission Line Type	Total Trace Length	Normal Impedance	Width & Spacing (mils)
H_A#[35..3]	Strip-line	0.5 - 6.5 inch	55 +/- 15%	W=4 & S=8 mils
H_REQ#[4..0]	Strip-line	0.5 - 6.5 inch	55 +/- 15%	W=4 & S=8 mils
H_ADSTB#[1..0]	Strip-line	0.5 - 6.5 inch	55 +/- 15%	W=4 & S=12 mils

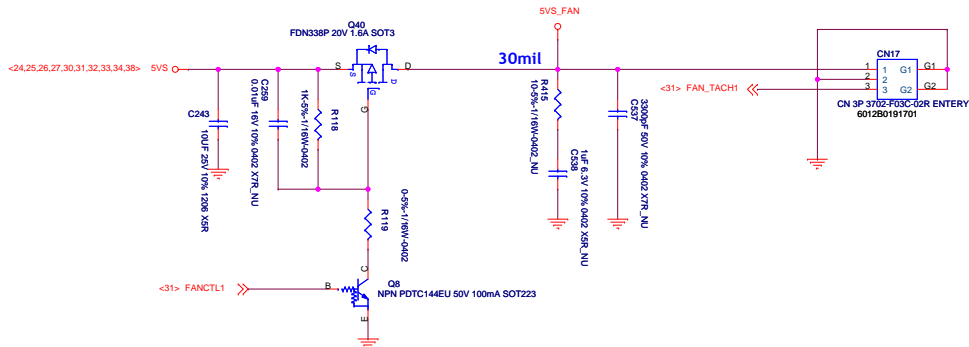


THERMAL SENSOR



B Change

Fan control

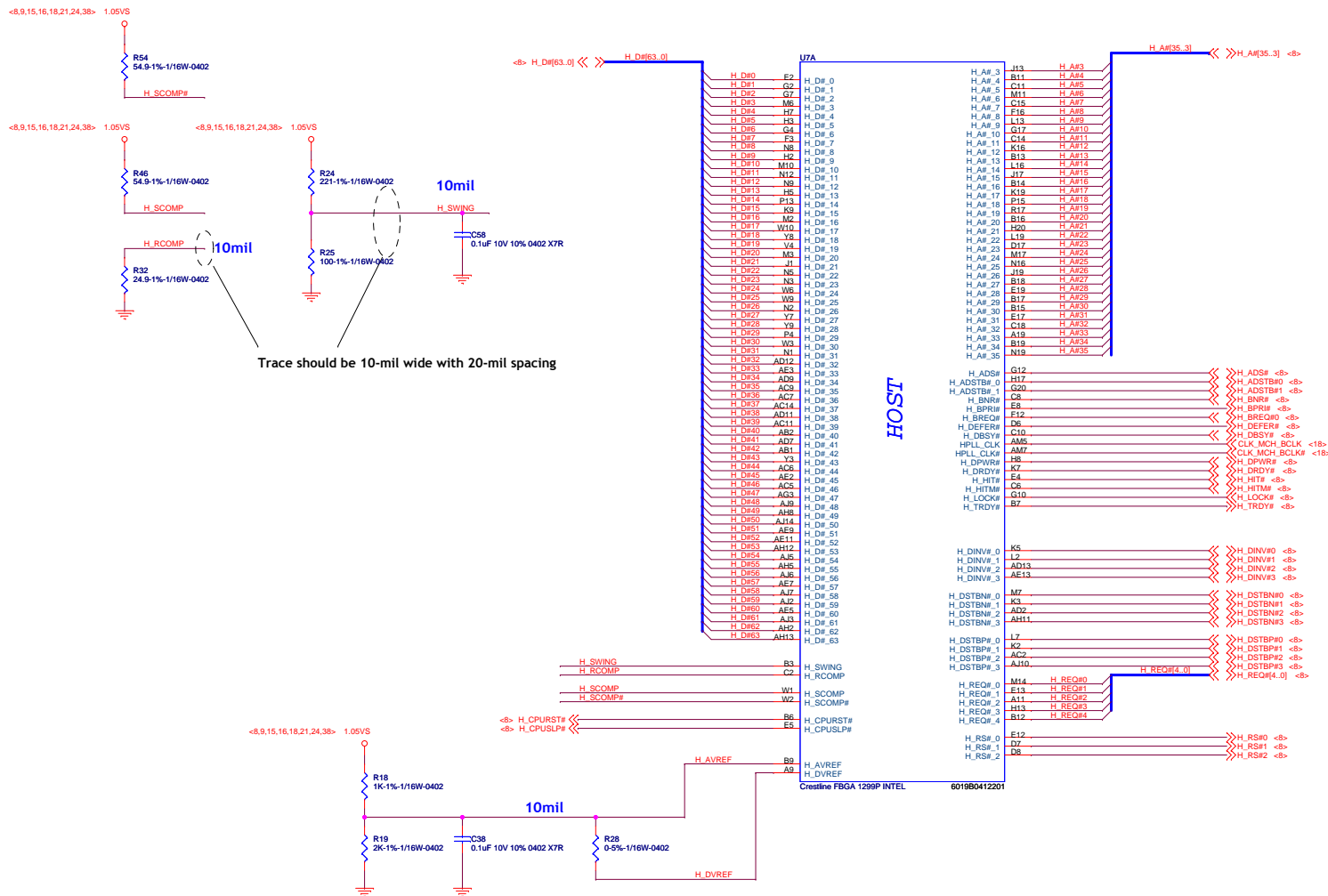


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Title		
M11D (Merom+Crestline+ICH8M)		
Size	Document Number	Rev

Size C	Document Number CPU Thermal	Rev AX1
Date: Friday, June 01, 2007	Sheet 11 of 43	



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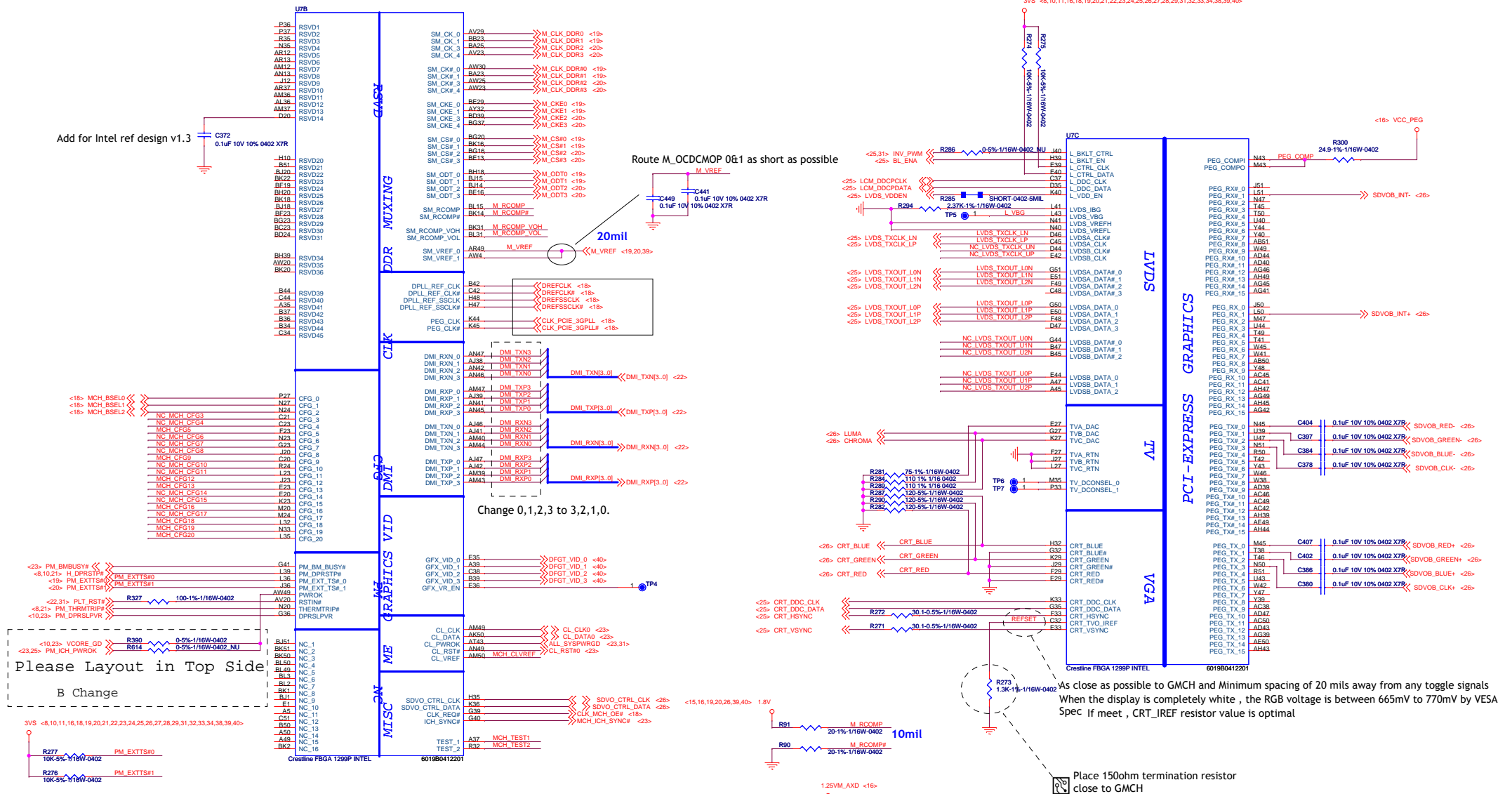
File

M11D (Merom+Crestline+ICH8M)

Crestline Host (1/6)

Rev AX1

Date: Friday, June 01, 2007 Sheet 12 of 43

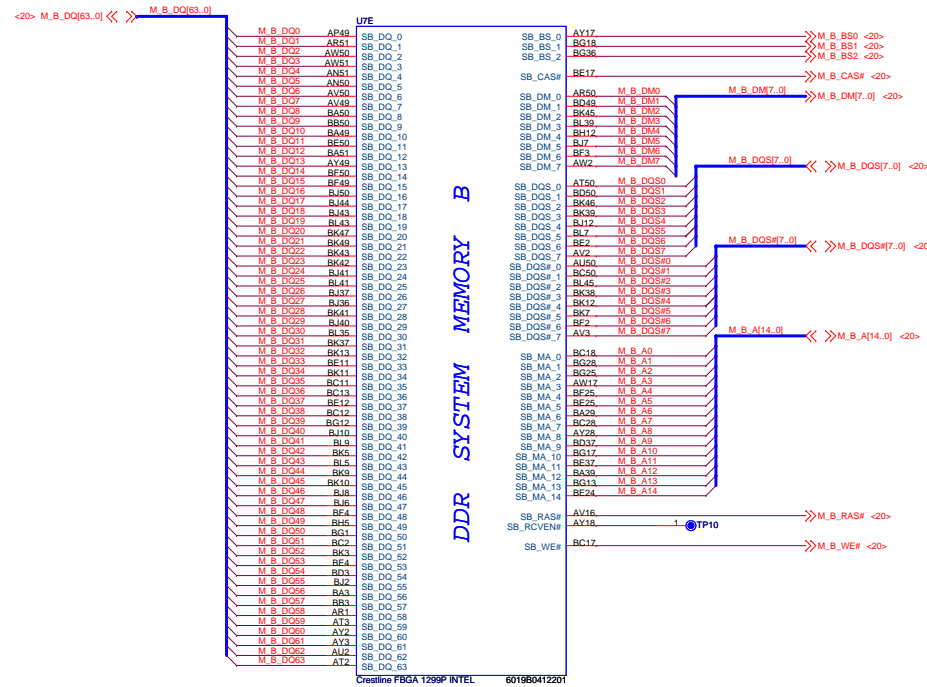
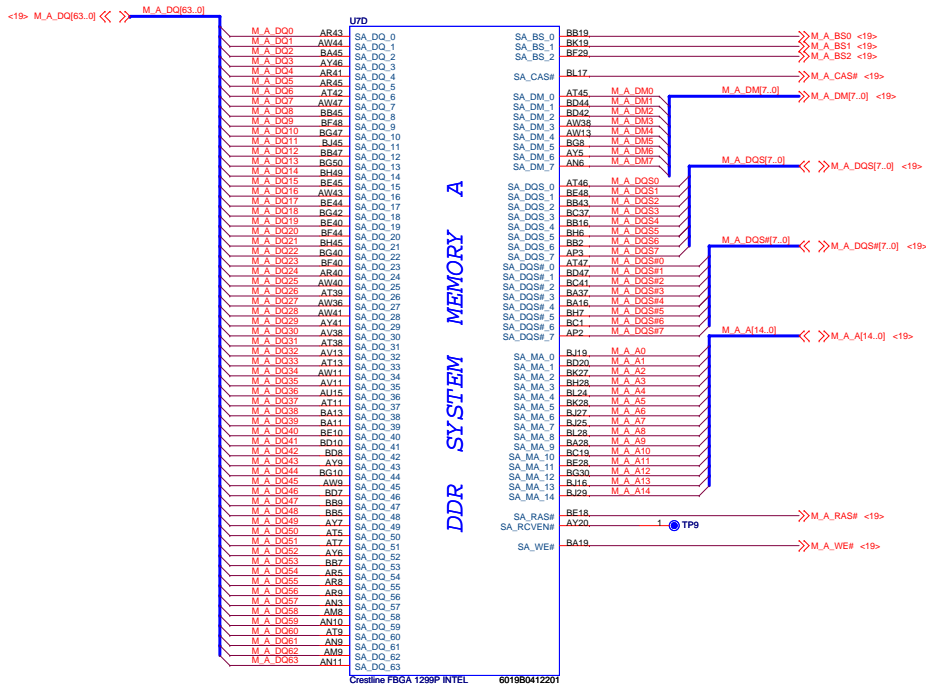


CRESTLINE (965GM) Strapping:

	Low	High
MCH_CFG5	Dmix2	Dmix4
MCH_CFG9 (PCIe Graphic Lane)	Reverse Lane	Normal Operation
MCH_CFG16 (FSB Dynamic ODT)	Dynamic ODT Disable	Dynamic ODT Enable
MCH_CFG18 (VCC Select)	1.05V	1.5V
MCH_CFG19 (DMI Lane Reversal)	Normal	Lanes Reversed
MCH_CFG20	Only SDVO or PCIE x1 is operation	Only SDVO or PCIE x1 with PEG port

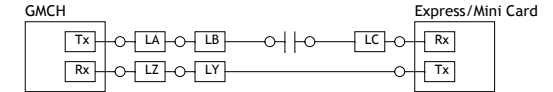
As close as possible to GMCH and Minimum spacing of 20 mils away from any toggle signals
When the display is completely white, the RGB voltage is between 665mV to 770mV by VESA Spec. If meet, CRT_IREF resistor value is optimal

Place 150ohm termination resistor close to GMCH



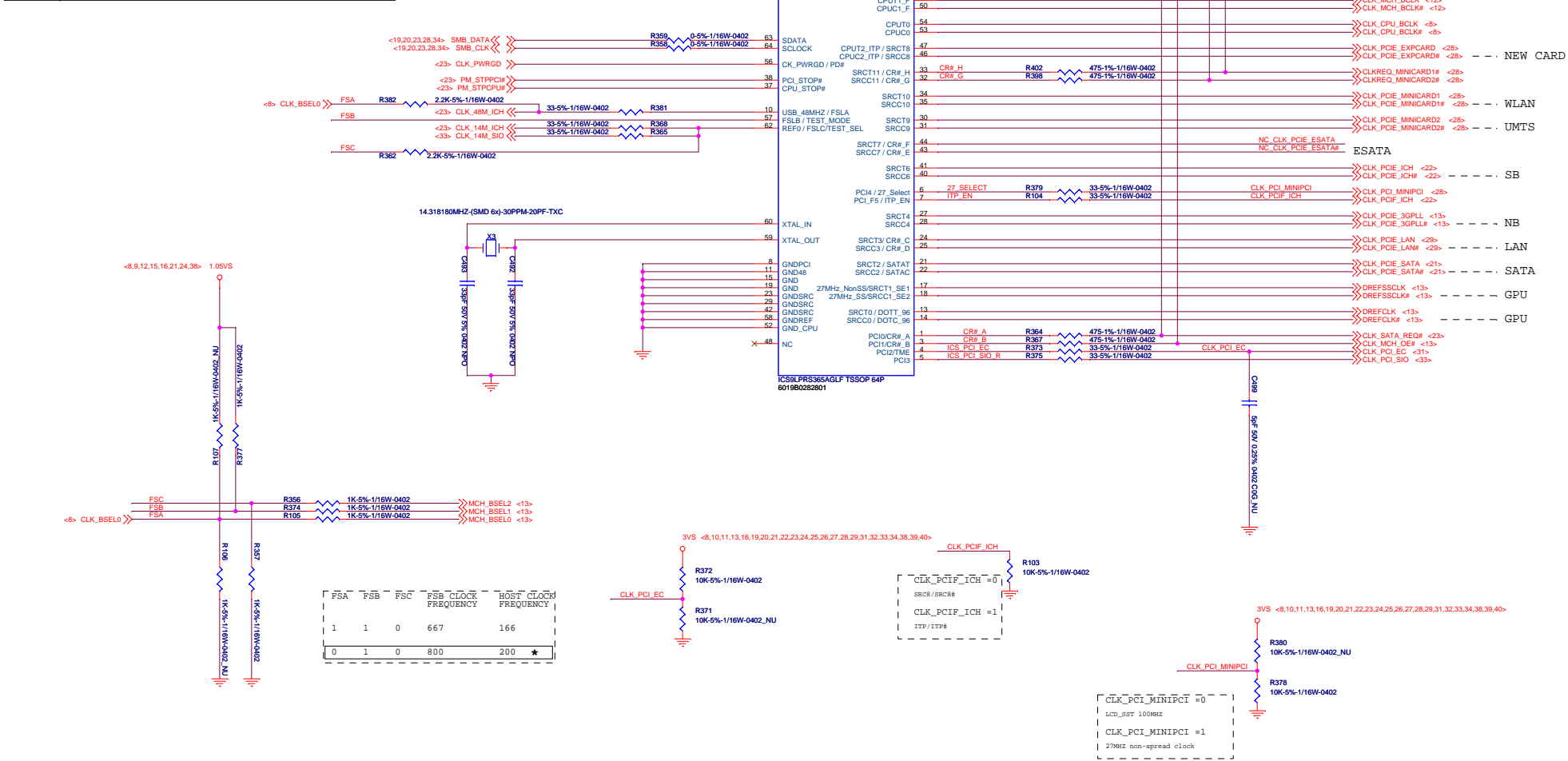

```

graph LR
    subgraph GMCH
        Tx1[Tx]
        Rx1[Rx]
    end
    subgraph ICH8m
        Rx2[Rx]
        Tx2[Tx]
    end
    Tx1 --- LA1[LA1]
    LA1 --- LA2[LA2]
    LA2 --- LB[LB]
    LB --- LC[LC]
    LC --- LD[LD]
    LD --- LE[LE]
    LE --- Rx2
    Tx2 --- LV[LV]
    LV --- LW[LW]
    LW --- LX[LX]
    LX --- LY[LY]
    LY --- LZ2[LZ2]
    LZ2 --- LZ1[LZ1]
    LZ1 --- Rx1
  
```



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Size C	Document Number		Rev AX1
Crestline Ground(6/6)			
Date:	Friday, June 01, 2007	Sheet	17 of 43

CR#_A:	Byte 5 bit 6=0--->SRC0 bit 6=1--->SRC2 bit 2=1--->SRC2	BIT 7=1 (Enable) BIT 3=1 (Enable)
CR#_B:	Byte 5 bit 4=0--->SRC1 bit 4=1--->SRC4	BIT 5=1 (Enable)
CR#_D:	Byte 5 bit 0=0--->SRC1 bit 0=1--->SRC4	BIT 1=1 (Enable)
CR#_E:	SRC6 (Byte 6)	BIT 7=1 (Enable)
CR#_F:	SRC8 (Byte 6)	BIT 6=1 (Enable)
CR#_G:	SRC9 (Byte 6)	BIT 5=1 (Enable)
CR#_H:	SRC10 (Byte 6)	BIT 4=1 (Enable)



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Date

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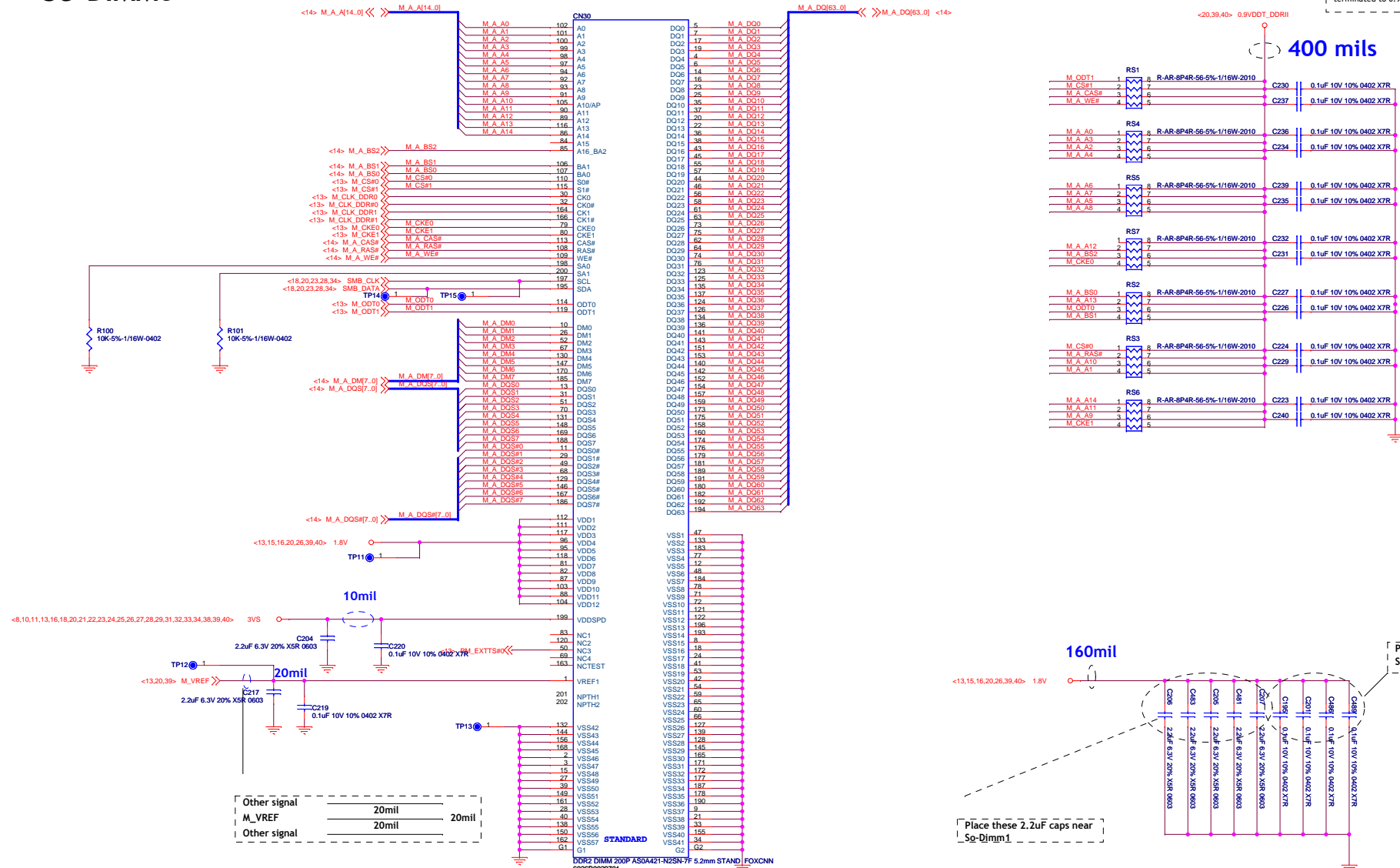
Clock Generator

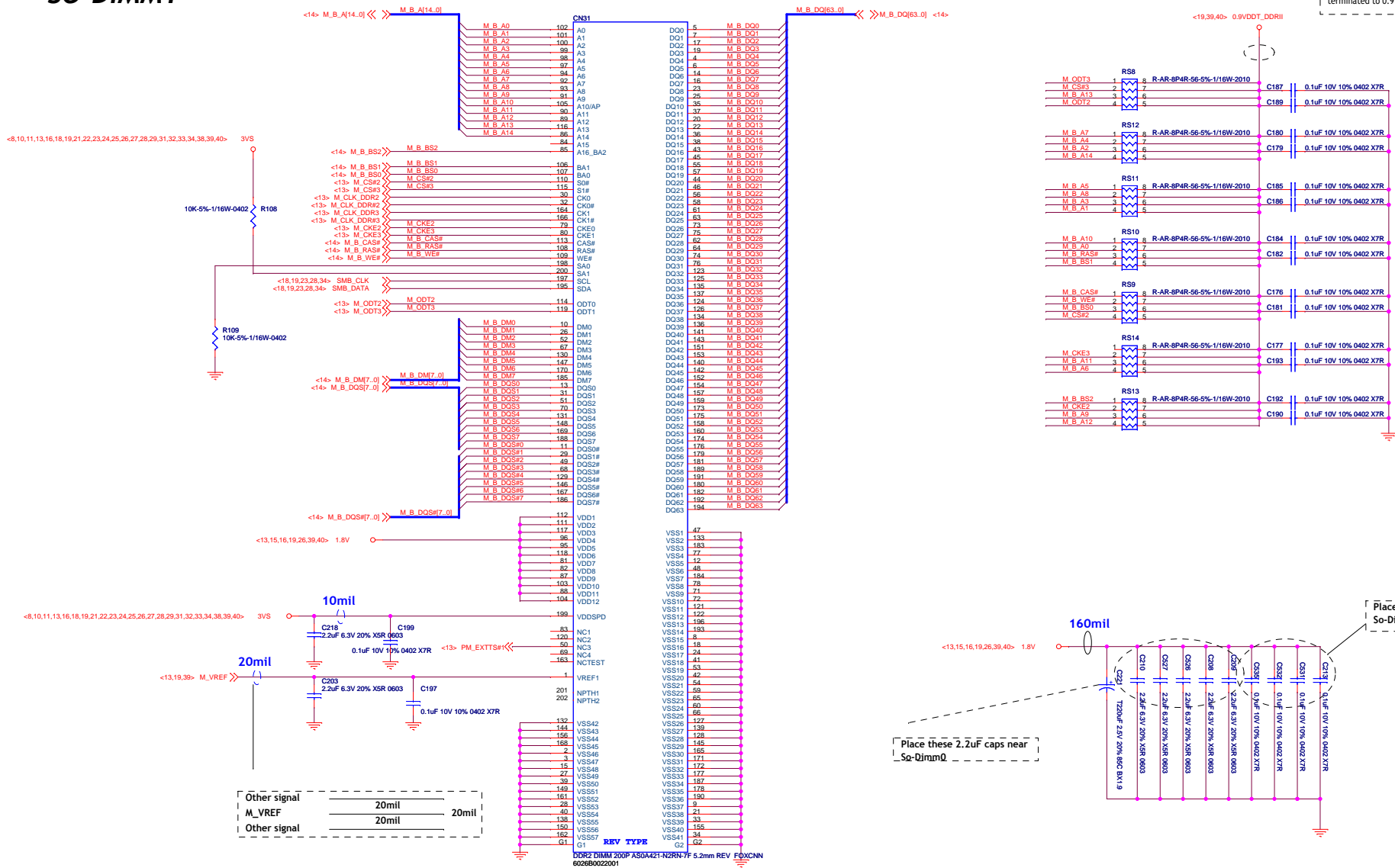
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AX1

SO-DIMM0

Place one cap close to every 2 pullup resistors terminated to 0.9VDDT_DDRII



SO-DIMM1

Place one cap close to every 2 pullup resistors terminated to 0.9VDDT_DDRII

Place these 0.1uF caps near
So-Dimm1 pin79-pin115 area

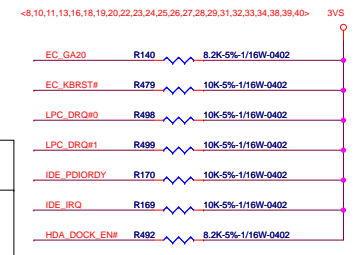
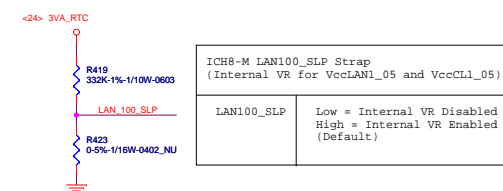
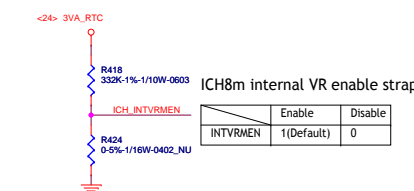
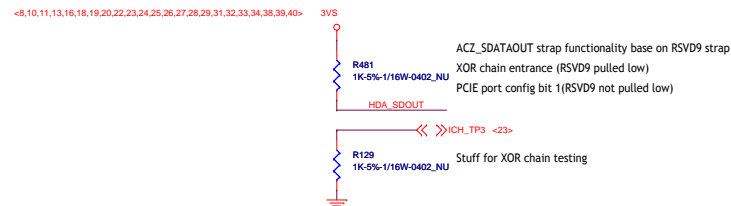
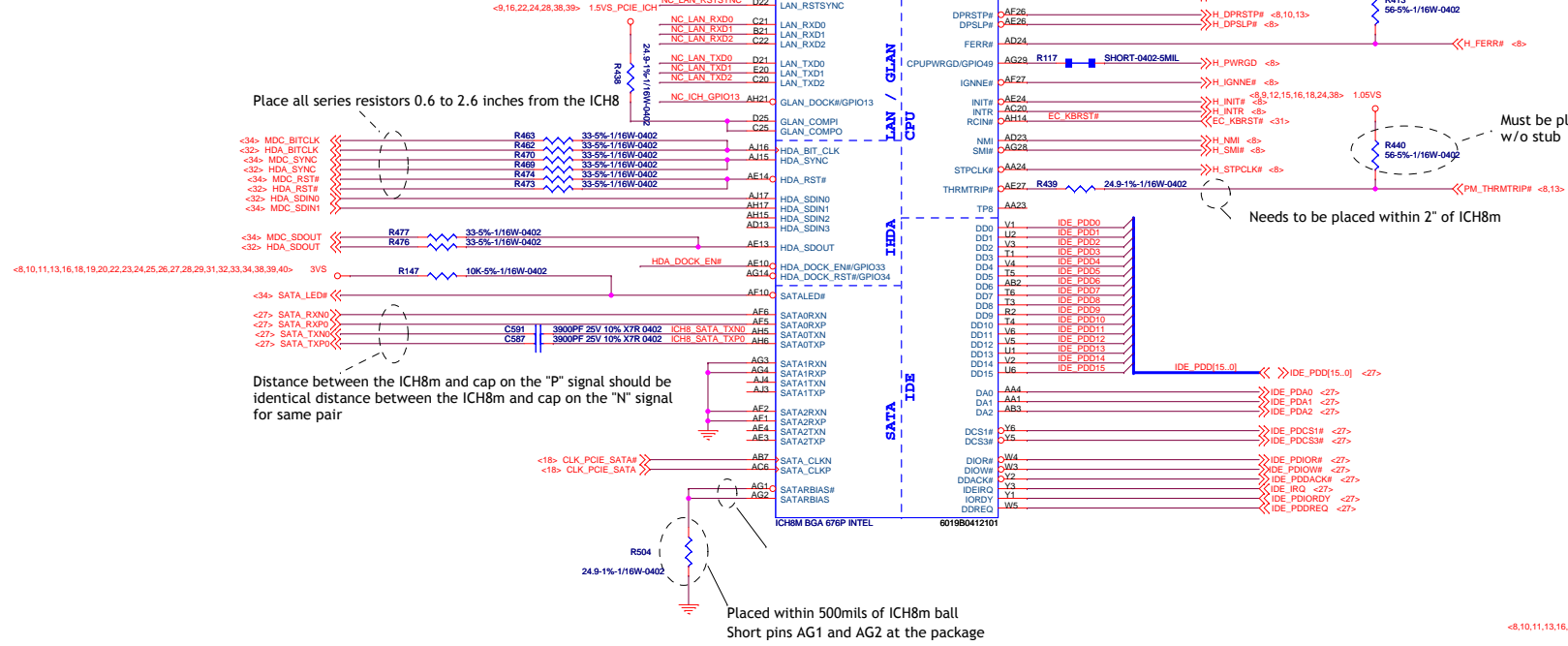
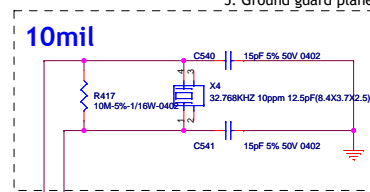
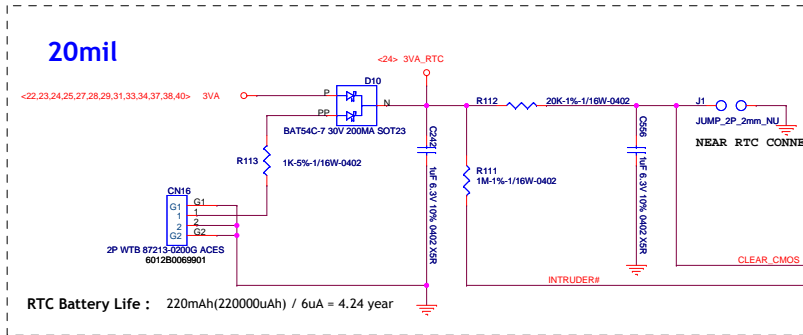
Place these 2.2uF caps near
So-Dimm0

RTC Circuit

1. RC delay time should be in the range of 18-25ms
2. It is recommended that this larger capacitor and small resistor value in order to reduce the likelihood of glitching of RTCRST#

RTC Crystal

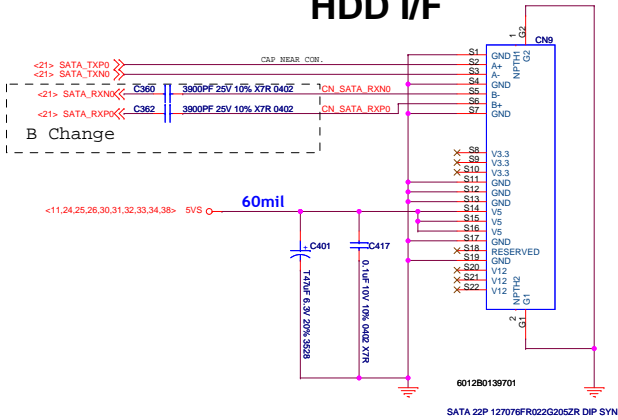
1. The ICH7m requires a length less than 1 inch on each branch (from crystal's terminal to RTCXn ball)
2. Routing the RTC circuit should be kept simple to simplify the trace length measurement and increase accuracy on calculating trace capacitances
3. On FR-4, a 5-mils trace has approximately 2pF per inch
4. Trace signal coupling must be limited as much as possible by avoiding the routing of adjacent PCI signals close to RTCX1 and RTCX2
5. Ground guard plane is highly recommended



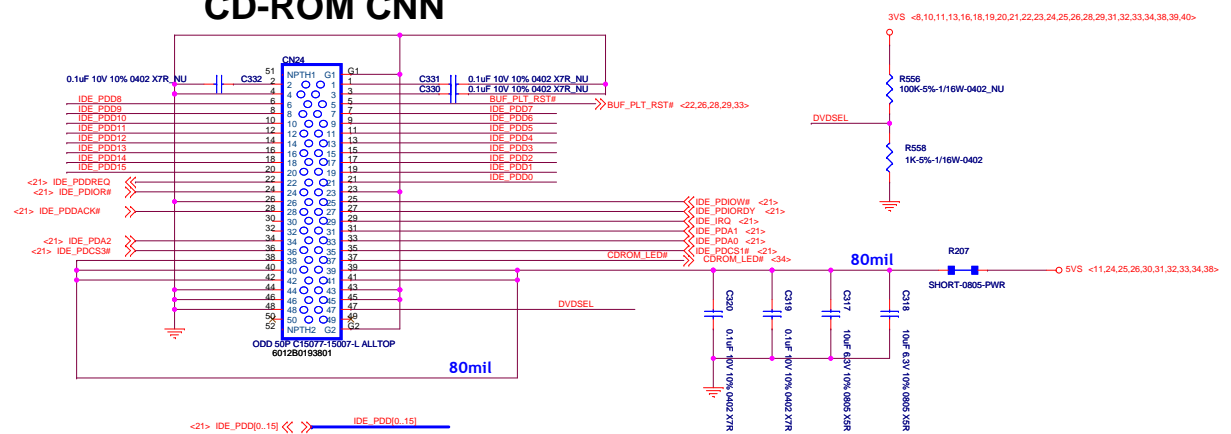
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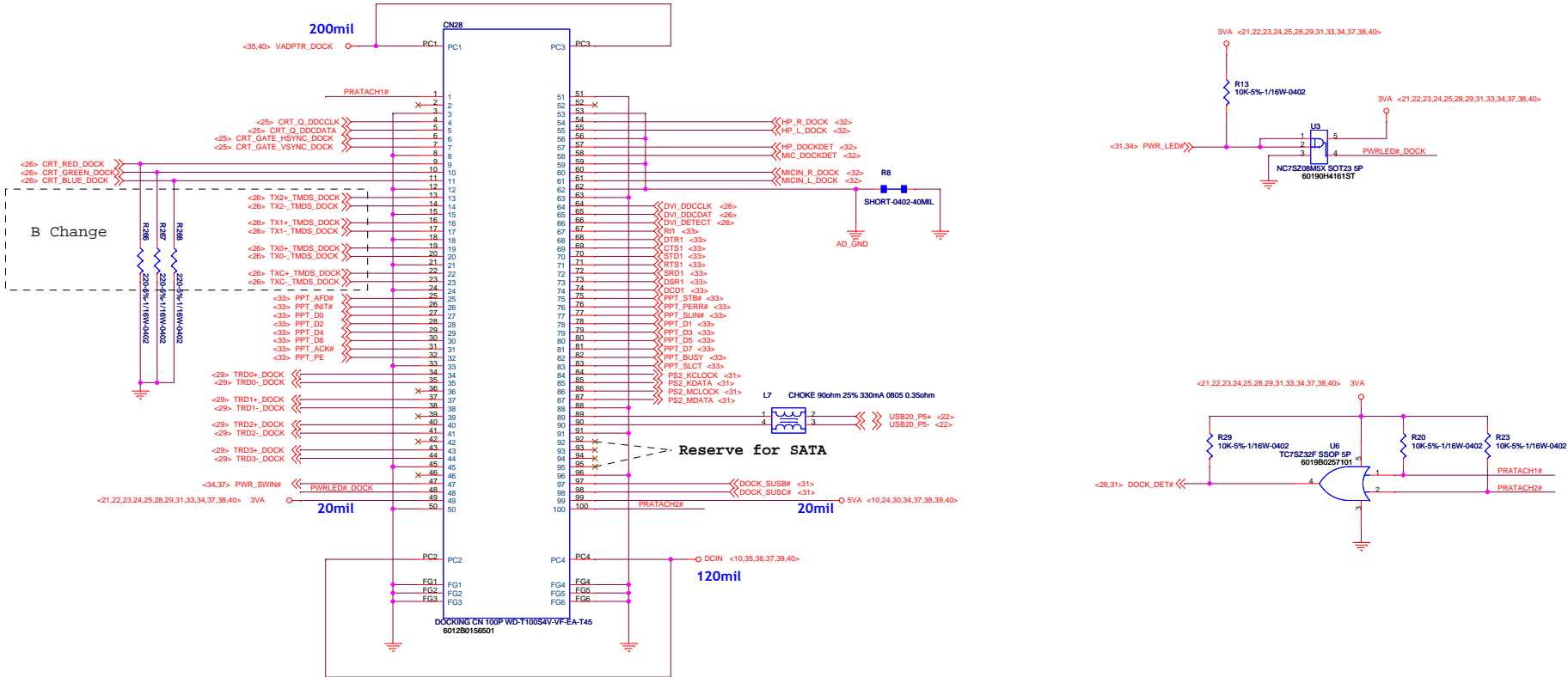
HDD I/F



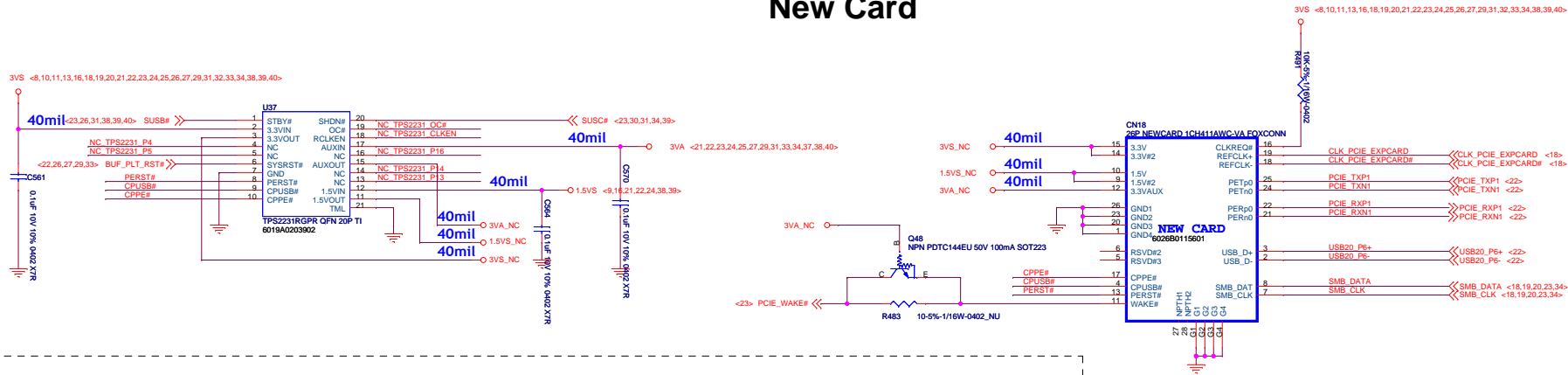
CD-ROM CNN



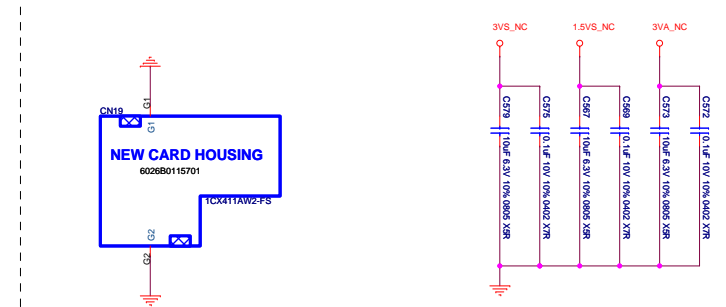
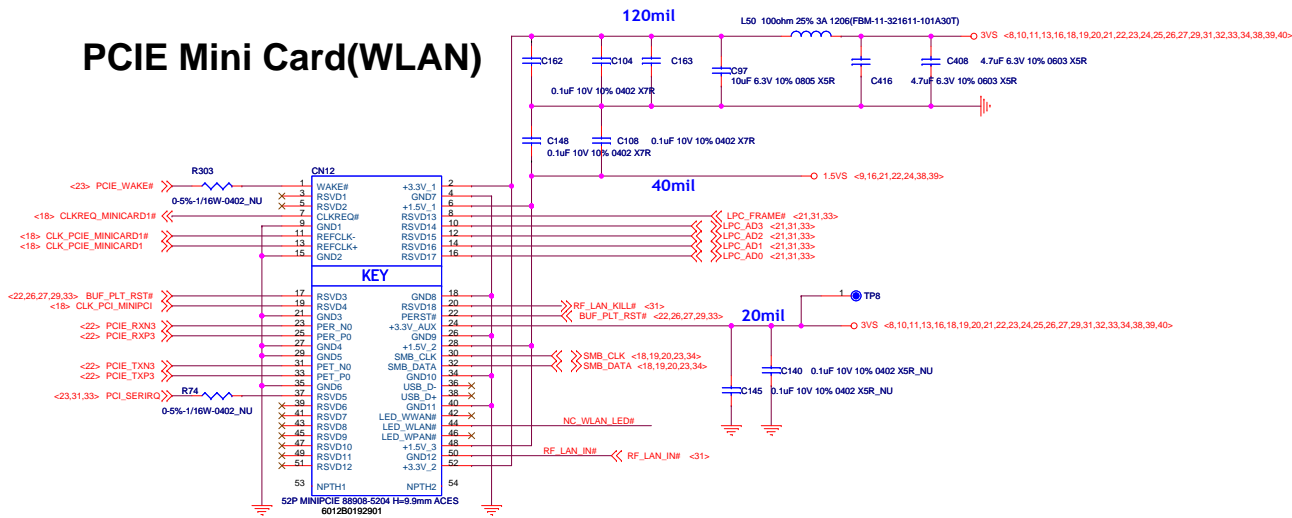
Docking CNN



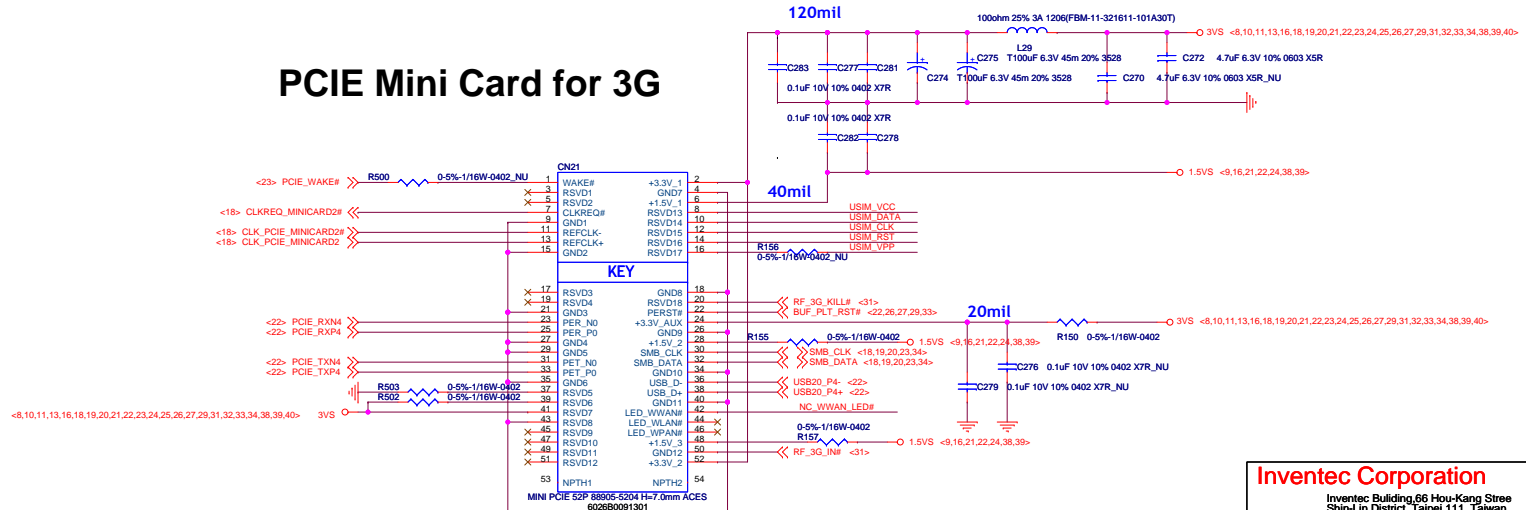
New Card



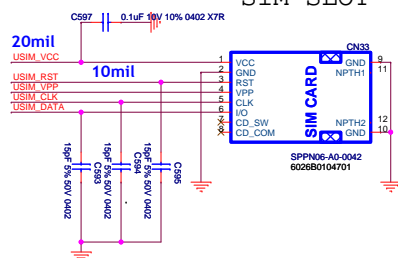
PCIE Mini Card(WLAN)



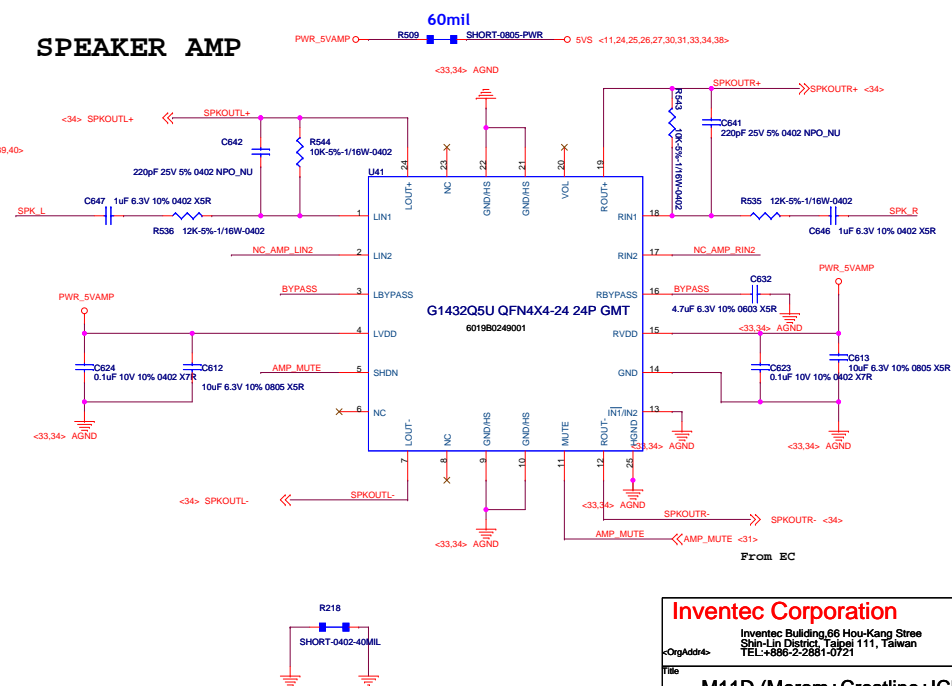
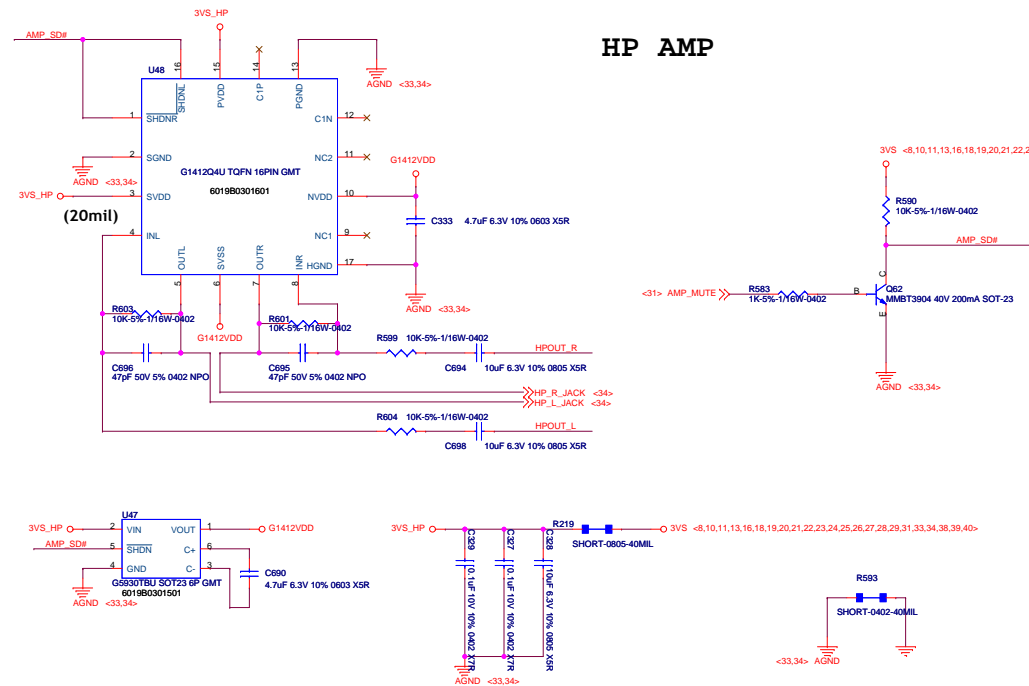
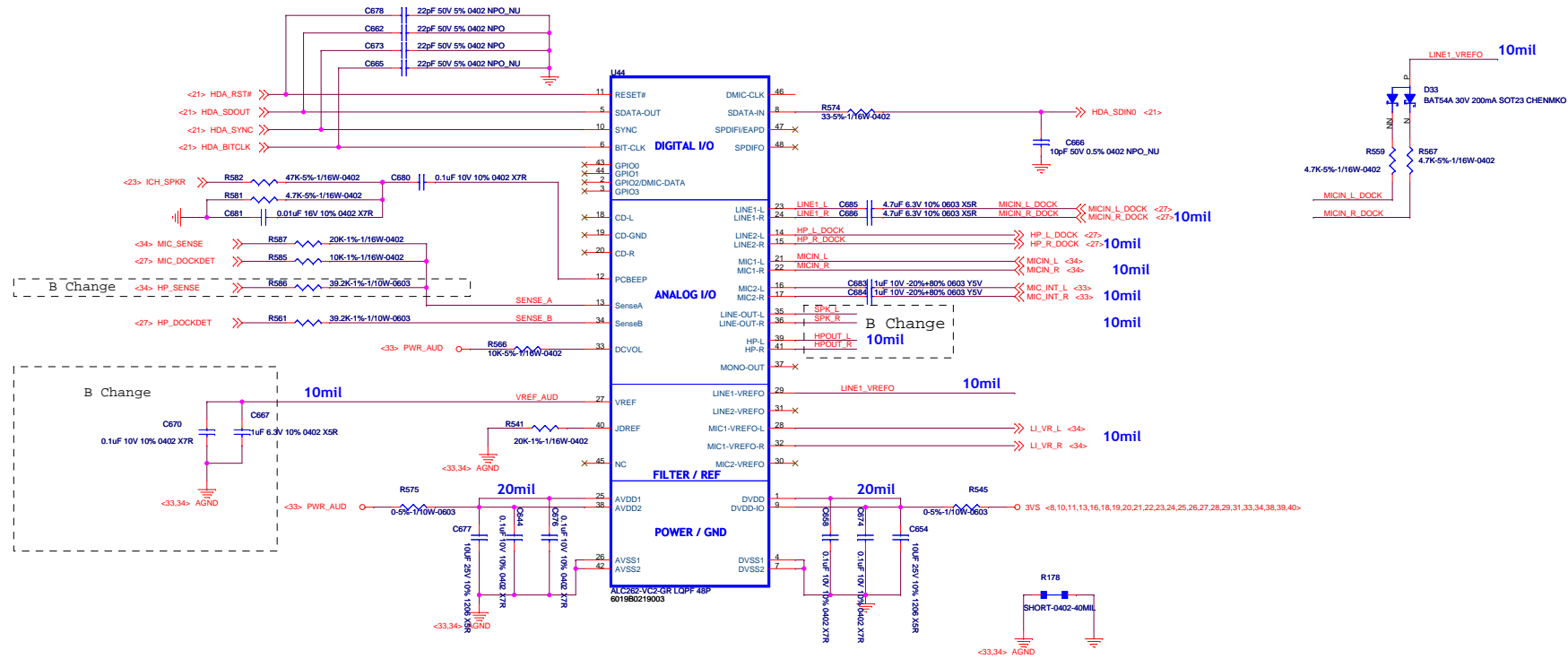
PCIE Mini Card for 3G



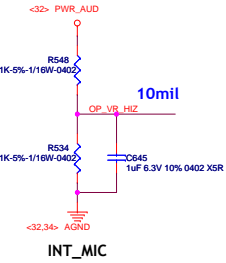
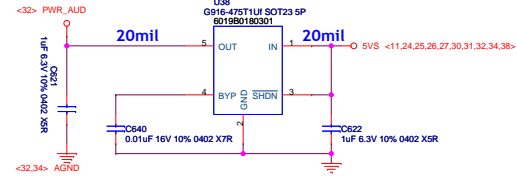
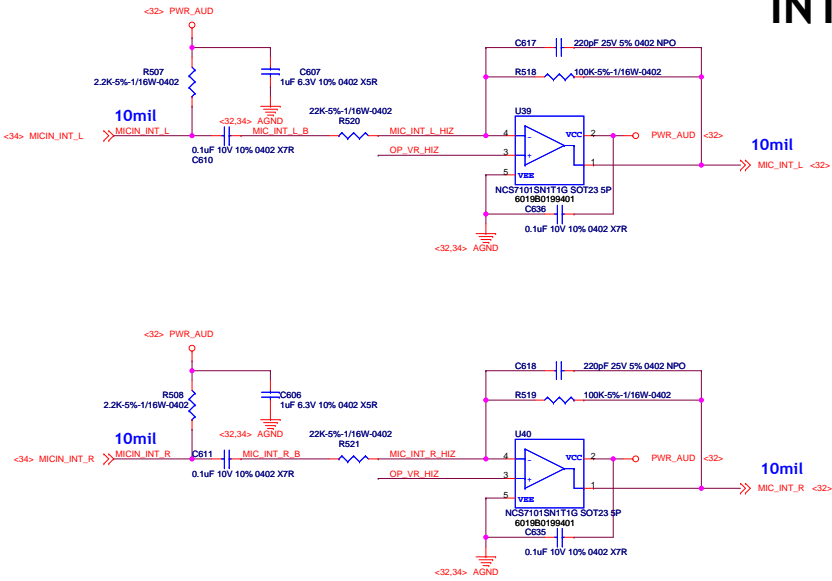
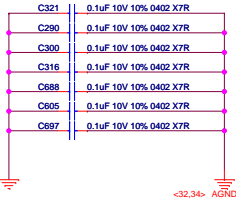
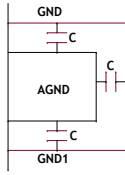
SIM SLOT



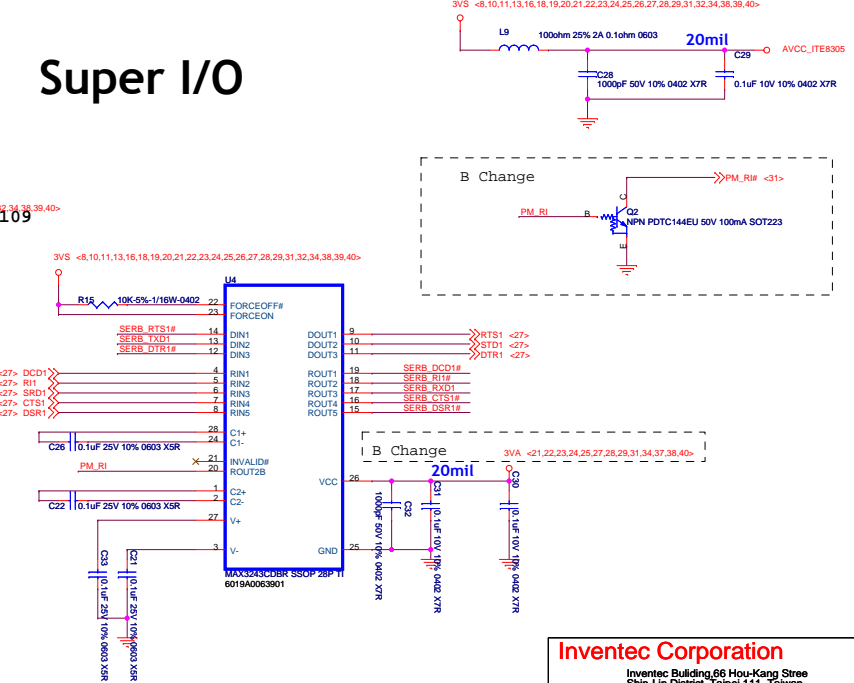
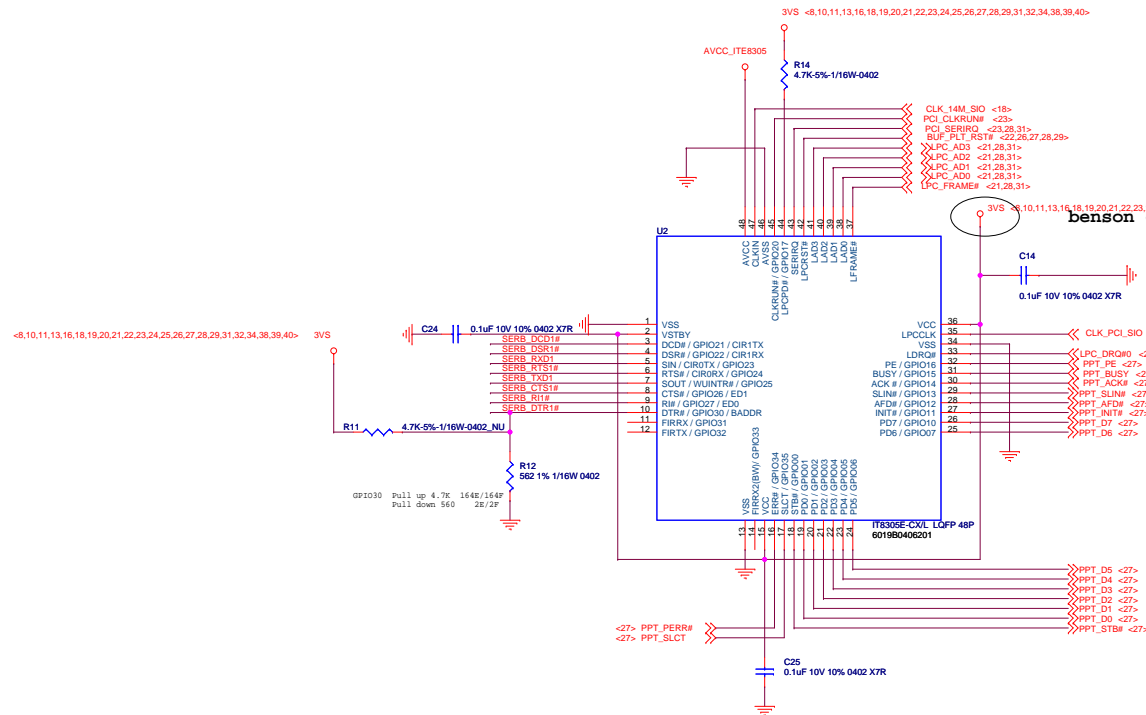


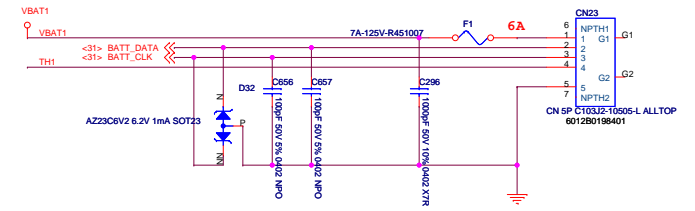
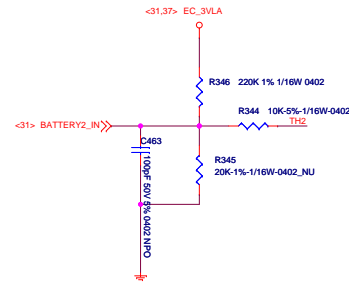
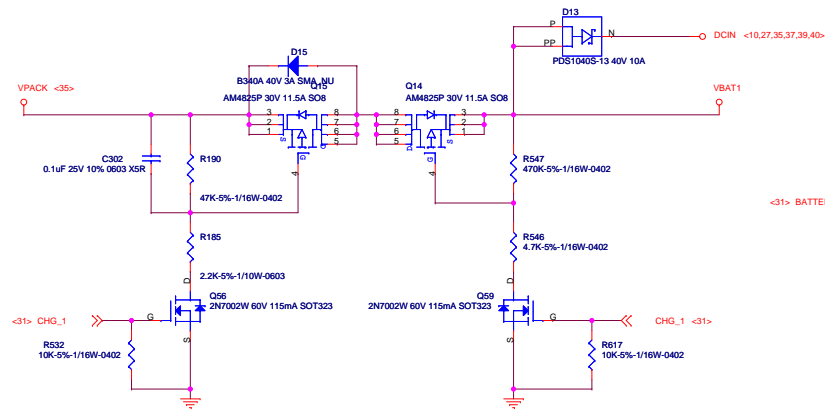


INT_MIC

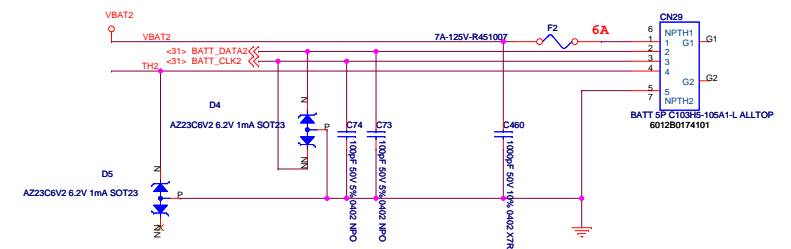
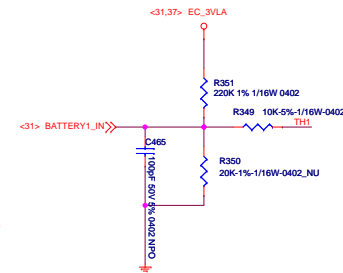
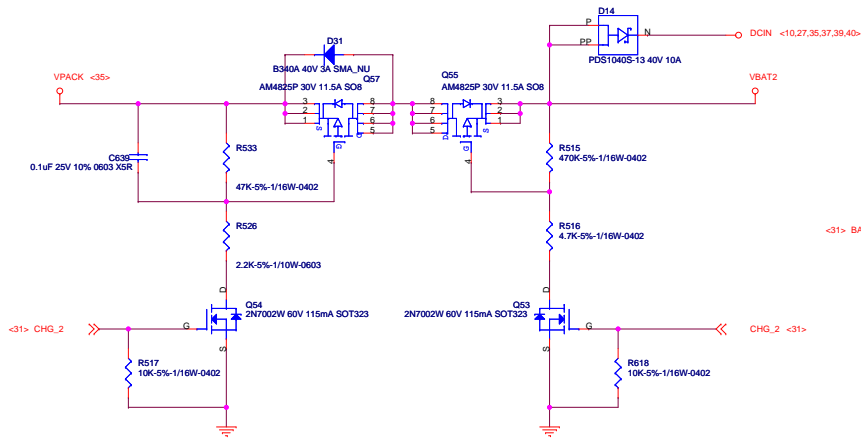


Super I/O

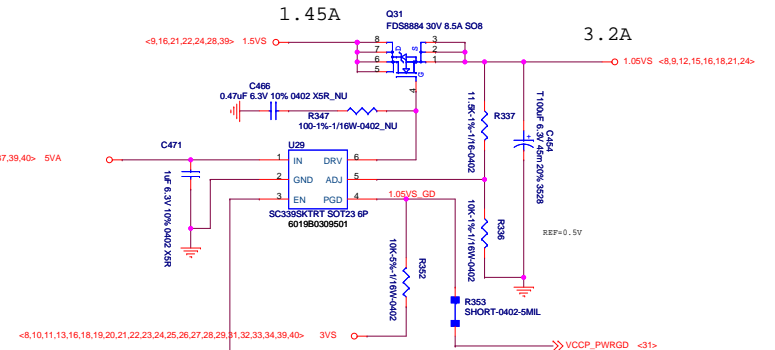
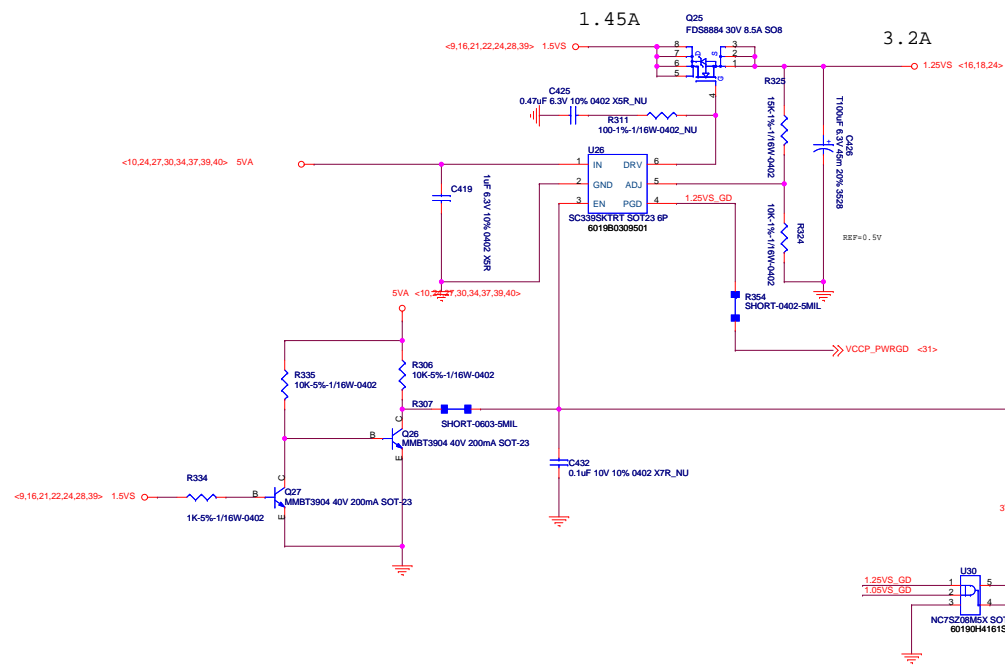
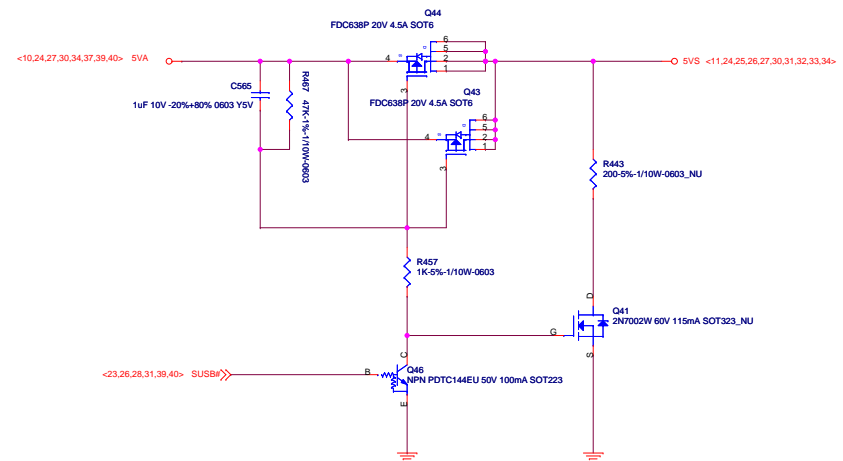
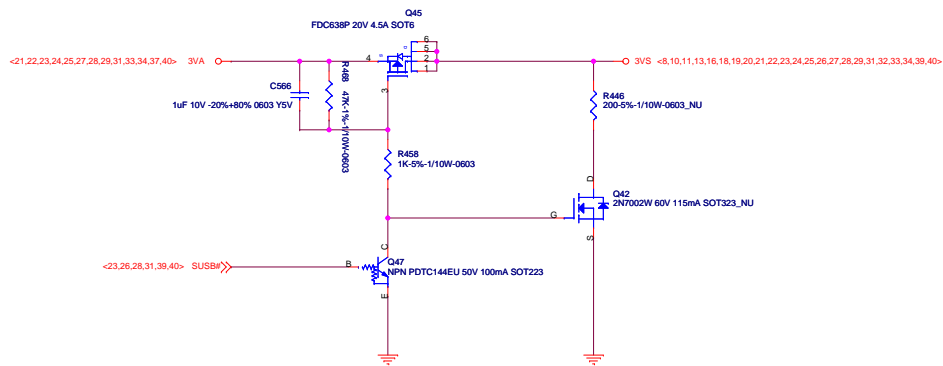


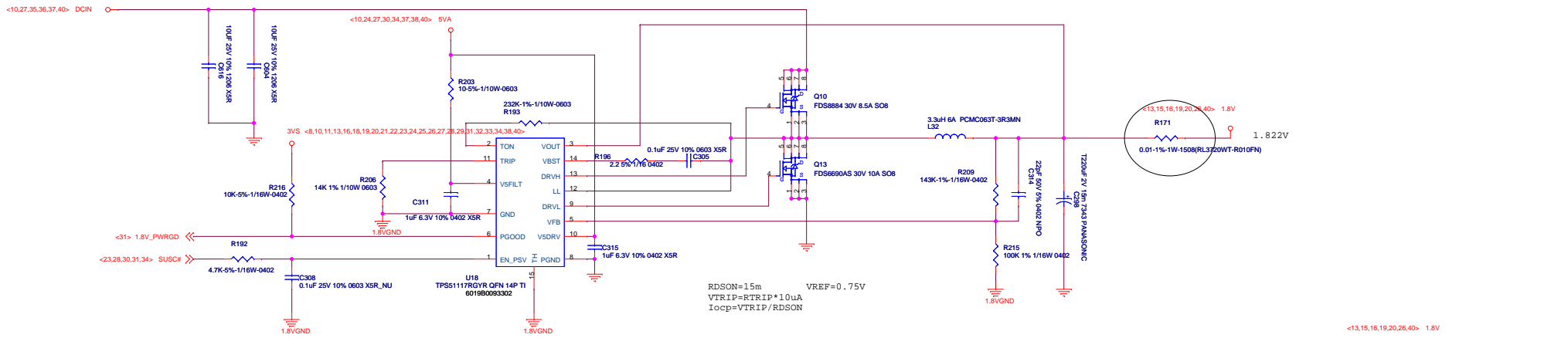


20mil

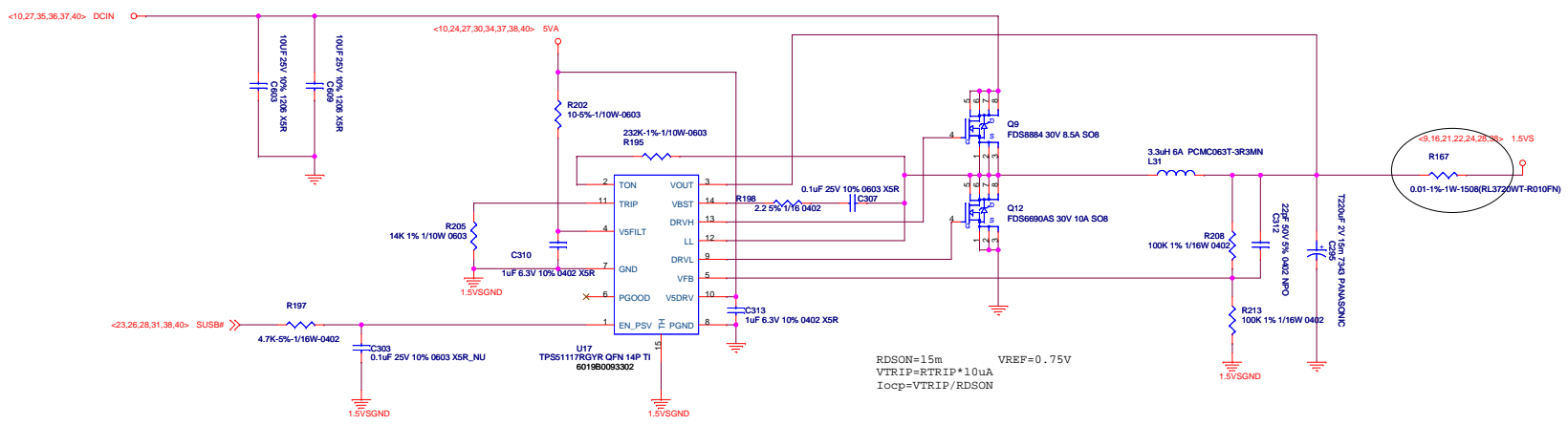
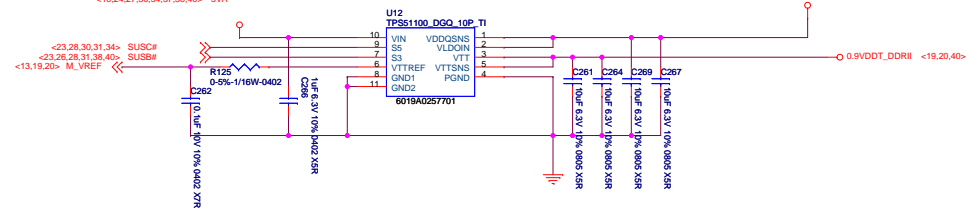


20mil



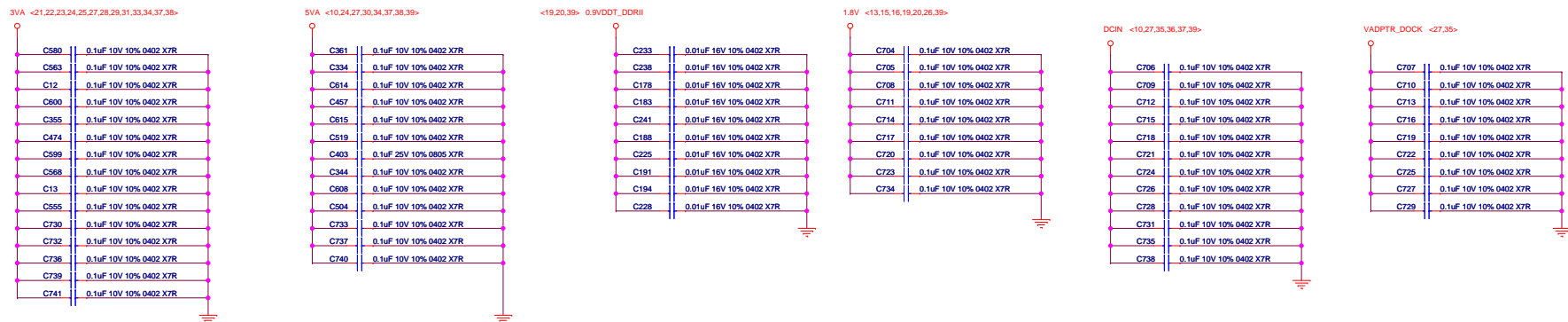
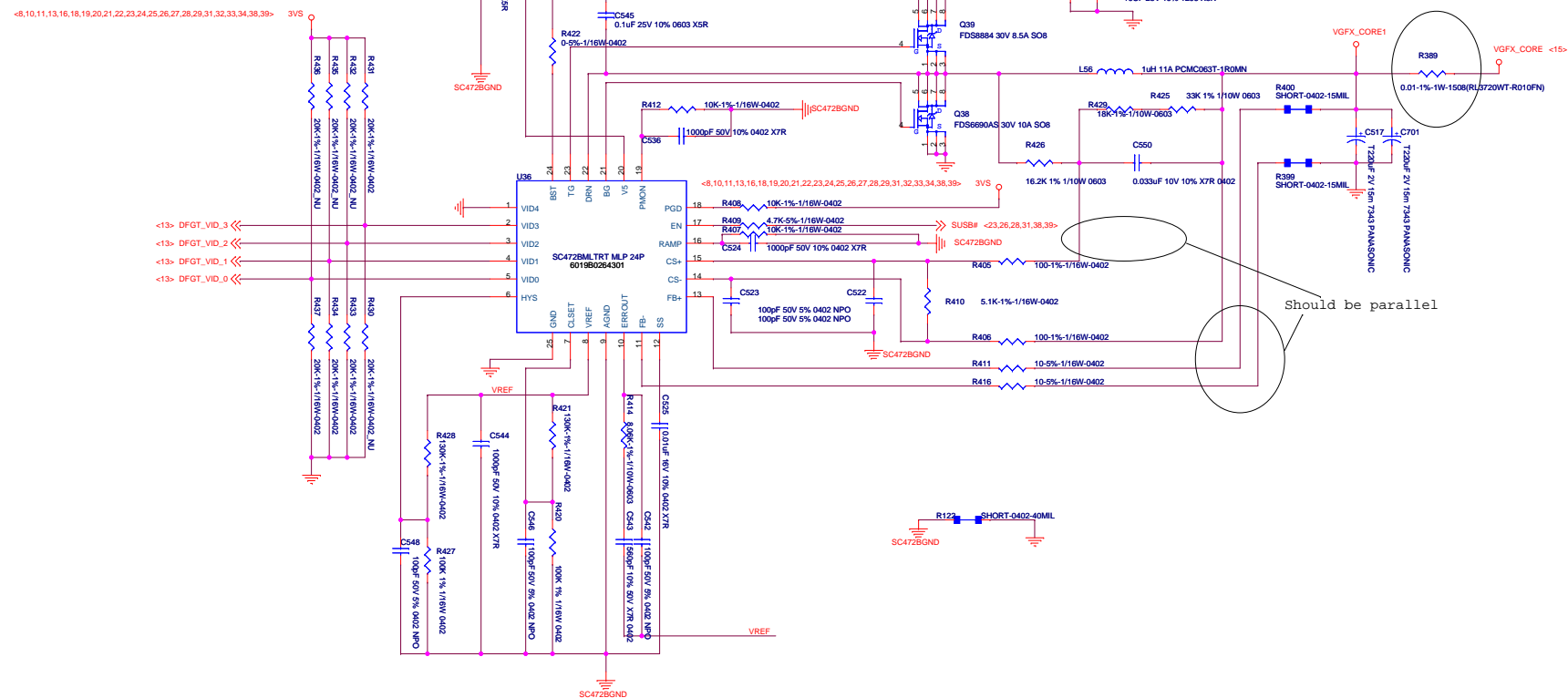


R217
 SHORT-0402-40MIL
 1.8VSGND
2 Vias **2 Vias**

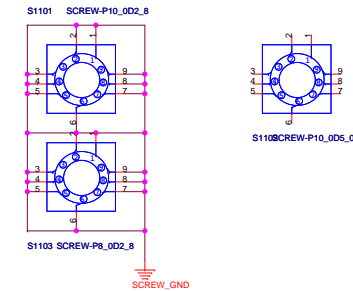
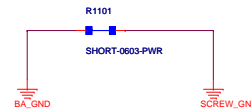
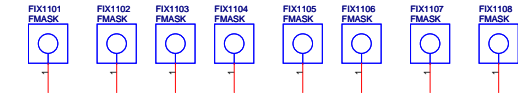
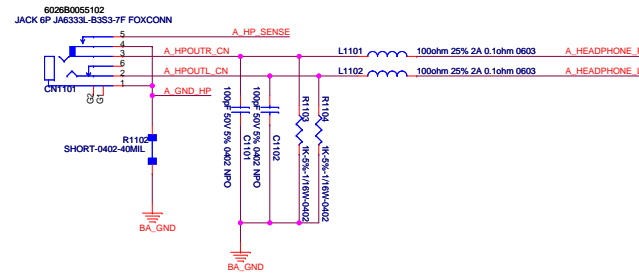
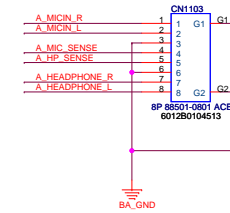
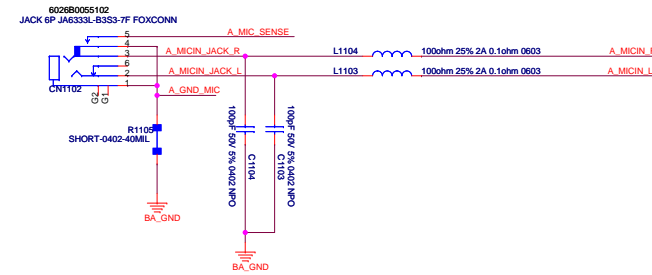


R214
 SHORT-0402-40MIL
 1.5VSGND
2 Vias **2 Vias**

GFX_CORE



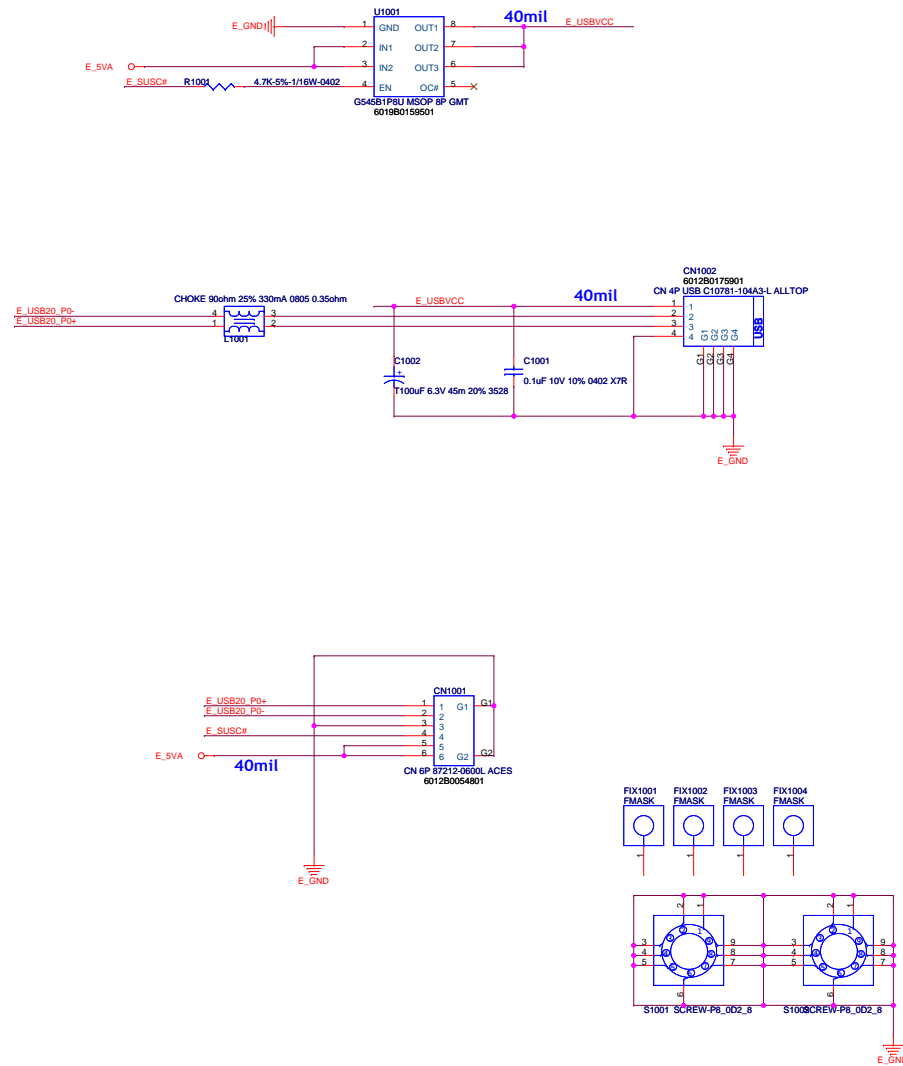
AUDIO BOARD



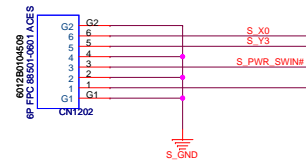
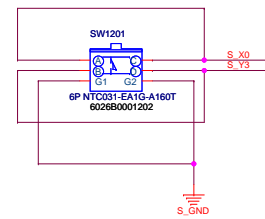
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File: **M11D (Merom+Crestline+ICH8M)**
Size: **Document Number**
Cusom: **AX1**
Date: **Friday, June 01, 2007** Sheet **41** of **43**

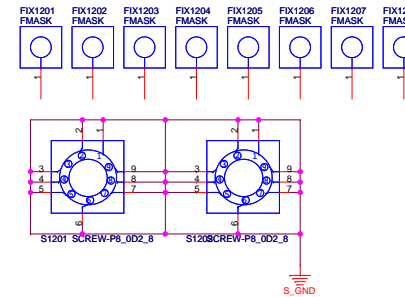
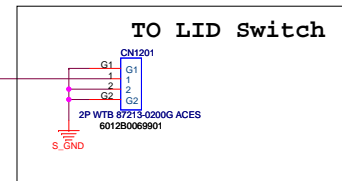
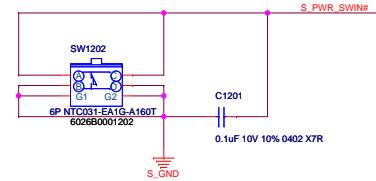
USB BOARD



WIRELESS LAN BUTTOM



POWER SWITCH

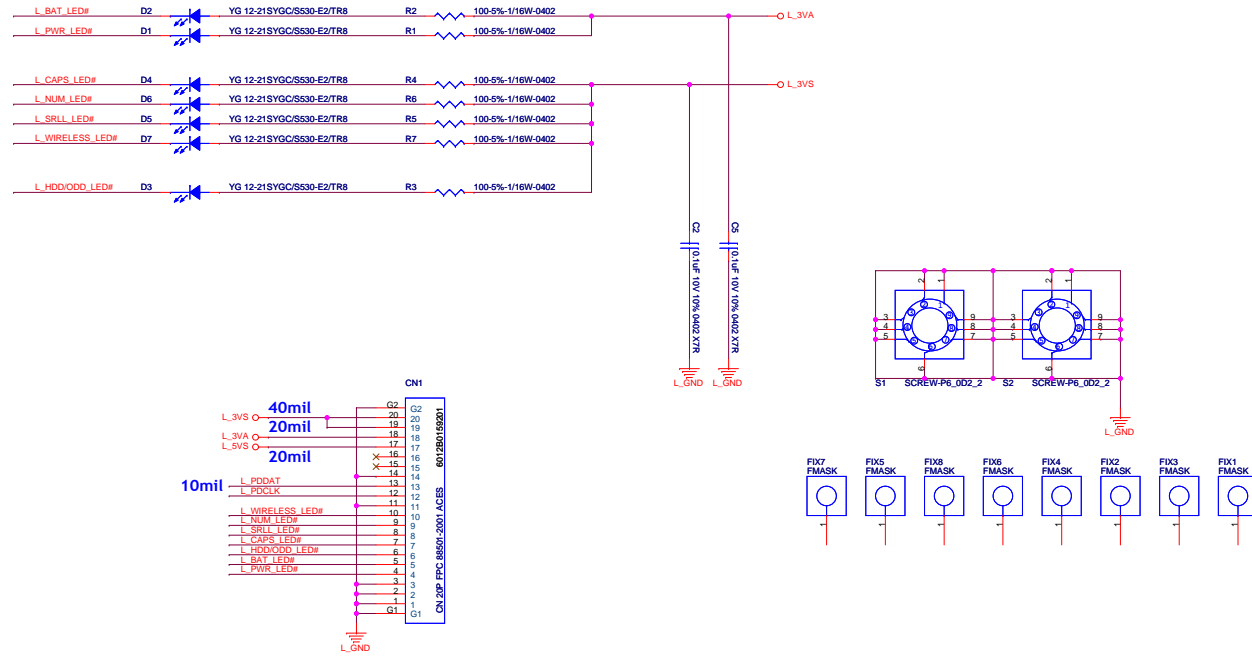


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Title		M11D (Merom+Crestline+ICH8M)	
Size	Document Number	Rev	
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Date: Friday, June 01, 2007		Sheet 43 of 43	

LED



GP CNN

